IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Gaetano Santoruvo et al.
Application No.	:	10/029,533
Filed	:	December 20, 2001
For	:	HEATING ELEMENT FOR MICROFLUIDIC AND MICROMECHANICAL APPLICATIONS
Examiner	:	Leonid M. Fastovsky
Art Unit	:	3742
Docket No.	:	01-RB-075 (850063.587)
Date	:	November 6, 2006

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Commissioner for Patents:

This brief is in furtherance of the Notice of Appeal, filed in this case on July 5, 2006. The fees required under Section 1.17(c), and any required request for extension of time for filing this brief and fees therefore, are dealt with in the accompanying transmittal letter.

I. REAL PARTY IN INTEREST

The real party in interest is STMicroelectronics, which is the assignee of the present invention.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which directly affect or will be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1, 4-8, 10-19, and 21-49 are pending. Claims 24-26, 28-30, 34, 35, and 42-49 are allowed; claims 1, 4, 5, and 16 are rejected; and claims 6-8, 10-15, 17-19, 21-23, 27, 31-33, and 36-41 are withdrawn pending allowance of a generic claim. All rejected claims are being appealed.

IV. STATUS OF AMENDMENTS

The Final Rejection was mailed April 5, 2006. In response to this Final Rejection, a Notice of Appeal was filed on July 5, 2006. No amendments have been filed in response to the Final Rejection of April 5, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The summary that follows is intended to provide a general description of the subject matter of the claims. The scopes of the respective claims are not to be construed by this summary.

The present invention relates to microchip heaters for microfluidic and micromechanical applications, such as integrated chemical microreactors for decomposition and detection of bioorganic compounds such as DNA, ink-jet printer heaters for firing ink for printing purposes, optical switching based on vapor bubble formation to deflect a light beam, and optical switching based on liquid crystals.[1]

A typical prior art device according to known technology employs one or more resistive heating elements to generate the heat for its operation. The heating element operation is controlled by one or more switching transistors to control electrical current in the element.[2] Such transistors can be either bipolar or MOS devices.

Transistors are known to produce heat when operating. One of the basic problems of integrated circuits over the last 20 years has been the heat generated by the transistors during

[1] Paragraph 2 of Patent Application Publication US2003/0116552A1, the published version of the present application, Appendix A, and cited herein as the '552 publication.

[2] Paragraph 10 of the '552 publication.

their normal operation. As the temperature of an integrated circuit increases, the performance of the individual transistors and the circuits decreases. The decrease in electrical performance is not linear with the temperature. For some circuits, a slight rise in temperature will such cause a marked decrease in electrical circuit performance, such that the circuit does not operate correctly. In addition, operation at excessive temperatures causes a greatly shortened life of the integrated circuit.

Great efforts are expended to keep the temperature of an integrated circuit within certain limits during normal operation. These efforts include the use of elaborate heat sinks, reducing the current consumption, using shallow junctions, reducing the total power that can be consumed within a certain time period. These efforts can be generally classified into two groups: removing the heat that is generated by the transistor operation and reducing the heat that is generated. All of these efforts are focused on one thing: keeping the transistor below a certain temperature range during operation.

The present invention takes a completely different approach. The present invention seeks to generate heat from a transistor. The goal of the present invention is to ensure that the operating temperate of the transistor is above a certain level. For the present invention to be used, the transistor itself must generate heat sufficient to raise its own temperature, and the temperature of surrounding material to higher than a selected level. This is so very different from any prior art uses of a transistor that not a single prior art reference discusses ensuring that the heat from the transistor is above a selected level and is high enough to achieve a desirable heating of an adjacent object. This is a new use for a transistor that is not present in any prior art reference. This is what is claimed in the present application.

A brief discussion of transistor operation, both MOS and bioplar, would be helpful. The term MOSFET, meaning *metal oxide semiconductor field effect transistor*, is commonly used to refer to a particular type of transistor formed in a semiconductor substrate. MOSFET transistors are controlled by varying a voltage potential at a *gate* terminal of the transistor, which in turn controls a charge concentration in a localized region, or *channel*, of the semiconductor substrate material. Where there is a high charge concentration, the channel becomes conductive, allowing electric current to flow across the channel. Thus, by regulating the voltage potential at the gate

terminal, electric current in the channel can be modulated or controlled as by a switch. Source and drain regions are conductive regions formed on either side of the channel and between which the current flows when the channel is conductive.

Bipolar transistors control the flow of electrons across a junction of two different types of semiconductor material. Bipolar transistors, as do other types of transistors, produce waste heat in response to current running through a region of the semiconductor, because of resistive properties of the material. These properties are not linear, which is acceptable for the present invention.

Pictured below is a sample transistor for use in the present invention, which can be either an MOS, bipolar or other transistor of the type commonly used in digital electronic devices. In the example shown, an MOS device is pictured, but the principles apply to other types of transistors.

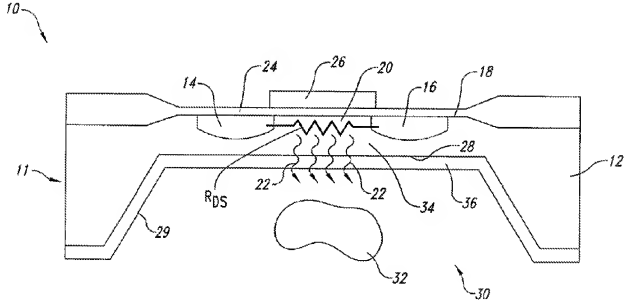

Figure 1.

Figure 1 is a copy of Figure 1 of the specification, and shows a fluid heater 10 according to an embodiment of the invention. The heater 10 is formed on a wafer 11 of semiconductor material such as, for example, silicon. The substrate 12 has been processed using well known MOSFET manufacturing techniques to form a source region 14 and a drain region 16 of a MOSFET in the substrate toward an upper side or surface 18 thereof. A channel region 20 of the

MOSFET transistor is formed in the substrate 12 between the source and drain regions 14 and 16 to conduct electric current between the source and drain regions. The channel region 20 is manufactured to have a selected resistance, indicated by a resistor symbol, to electric current so as to generate heat, indicated by arrows 22, when conducting electric current.[3]

A dielectric layer 24, for example an oxide, is formed on the upper side of the substrate 12 and extends across the channel region 20. A gate electrode 26 of the MOSFET is formed by a layer of metallization disposed on the dielectric layer 24 above the channel region 20 to control the current conducted by the channel region between the source and drain regions. The MOSFET can be of any suitable type, such as LDMOS, VDMOS, etc.[4]

A lower side or surface 28 of the substrate 12 has a portion thereof below the channel region 20, at the back of the wafer 11, etched away or otherwise removed to reduce the thickness of the substrate in this area and to form a recess 29 in the substrate. The recess 29 defines, at least in part, a chamber 30 that is heated by heat 22 generated by the channel region 20. The chamber 30 may be sized and shaped to receive a substance 32 to which the heat 22 transmitted into the chamber 30 is transferred. The chamber 30 is positioned close to the channel region 20 to receive the heat 22 generated by the channel resistance R_{DS} when the channel region is conducting electric current. A portion of the substrate 12 is removed when forming the chamber 30 so as to leave only a thin wall portion 34 thereof remaining below the channel region 20 in order to have the heat source (*i.e.*, the channel region) close to the substance 32 to be heated.[5]

A dielectric layer 36 is formed on the lower surface of the substrate 12 so as to line a portion of the recess 29. This may be for the purpose, for example, of preventing fluids that are heated in the recess from chemically reacting with the material of the substrate, or from acting as a conductor and affecting the electrical properties of the device. The dielectric material is selected to be thermally conductive to permit transmission of thermal energy from the channel region 20 to the recess 29.[6]

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[3] Paragraphs 30 and 35-37 of the '552 publication 0030 and 0035-0037.

[4] Paragraph 31 of the '552 publication.

[5] Paragraph 32 of the '552 publication.

[6] Paragraph 33 of the '552 publication.

In the manufacture of typical MOSFET devices, the channel region is formulated to have as little resistance as possible when the device is fully conducting. This reduces thermal losses during operation, and minimizes the need for external cooling of such devices. In contrast to this general rule, the channel region 20 of the present invention is formulated to have a resistance that will be capable of producing a desired amount of heat in response to a given current in the channel region.

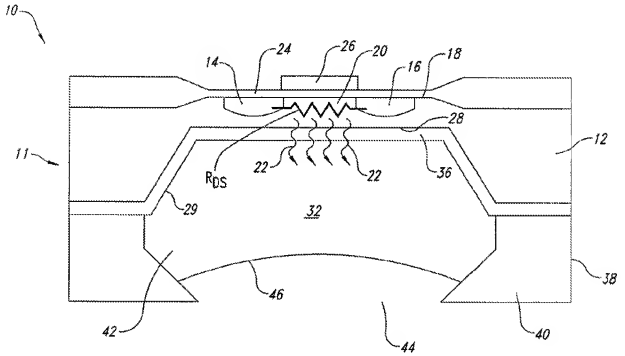

Figure 2.

Figure 2 is a copy of Figure 2 of the specification, and shows an embodiment that is substantially similar to that described with reference to Figure 1 of the specification. The heater 10 of Figure 2 has the same basic construction as the heater of Figure 1 except that the chamber is in part formed by a body 38 that has a wall portion 40 that extends about the recess 29 in the substrate 12 on the back of the wafer 11. The wall portion 40 of the body 38 is positioned adjacent to and in sealing engagement with the substrate 12 at its lower side 28, with the dielectric layer 36 positioned therebetween. The wall portion 40 defines an open interior portion

42 that mates with the recess 29 to form the chamber 30, and defines an orifice 44 through which the substance 32 can pass, which in Figure 2 is shown as a fluid with a meniscus 46.[7]

VI. GROUNDS OF REJECTION TO BE VIEWED ON APPEAL

1. Should claims 1, 4, 5, and 16 be rejected under 35 U.S.C. § 102(b) as being anticipated by Cozad, U.S. Patent No. 6,160,243 (the Cozad '243 patent).

VII. ARGUMENT

Prior to addressing the claim rejections, and in order to simplify the discussion of the rejections, applicants wish to discuss some aspects of U.S. Patent No. 6,160,243 to the Cozad '243 patent,[8] which is the sole reference relied upon by the Examiner in rejecting the claims. A copy of the Cozad '243 patent is provided as Appendix B of section IX of this brief.

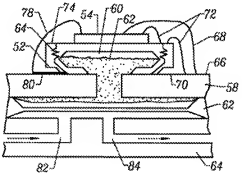

Figure 3.

Cozad is directed generally to thermally conductive fluid boilers. Figure 3 is a copy of Figure 4 of the Cozad '243 patent, and shows an embodiment in which a boiler 52 is positioned on an insulating substrate 58, and has an external heater 54 incorporated with the boiler 54. A resistive heater 54 provides thermal energy to the boiler.

> The external heater 54 provides a resistive heat source. Preferably, the external heater 54 includes a control circuit to reduce heat output from the heater 54 when the heat output reaches a predetermined temperature. Alternately, the external heater 54 includes a control circuit to reduce current flow through the heater 54 when the current flow reaches a predetermined value. By way of example, the

[7] Paragraph 42 of the '552 publication.

[8] Hereafter the Cozad '243 patent.

external heater 54 has been implemented with a MC7805 integrated circuit sold by Motorola, Inc., Schaumburg, Ill.[9]

The Cozad '243 patent does not provide any further discussion with regard to the resistive heater or control circuit of the heater 54, and depicts the heater as a block in circuit diagrams of Figures 5, 7, 9, and 11. Thus, the only teaching provided by the Cozad '243 patent with regard to the actual structure of the heater 54 is such information as may be available with regard to the Motorola MC7805[10]. The Cozad '243 patent does not provide a detailed diagram or explanation as to how the device is configured to control operation in response to the heat output.

Of some importance, the Cozad '243 patent itself stated, as quoted above that the current flow is limited to reduce the heat from its external heater 54. The data sheet of the MC7805 has a number of references to providing thermal overload protection and shut down of the circuit if it exceeds a certain value.[11] There is no discussion of the requirement that the heater itself, much less the transistors controlling it, must reach above a selected temperature.

A separate load resistor is provided, and while its operation is not fully explained either, one of ordinary skill in the art would understand that such a resistor might serve to establish a desired current or voltage of the device. An example of one such circuit can be found at Figure 7 of the Motorola datasheet of Appendix C.

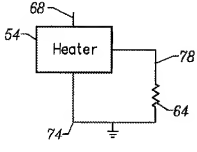

Figure 4

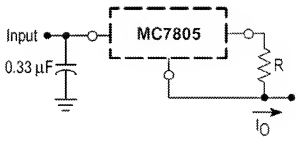

Figure 5

Figure 4 is a copy of Figure 6 of the Cozad '243 patent, and Figure 6 is a copy of Figure 7 of the Motorola data sheet, which provides a current regulator configuration. A comparison of

[9] Cozad, column 3, lines 54-62.

[10] Motorola MC7800/D datasheet is included as Appendix C in section IX of this document.

[11] Motorola MC7800/D datasheet page 1, first paragraph, page 13, Figure 4, page 14, first paragraph.

the diagrams of Figures 4 and 5 show a substantially identical configuration. In this arrangement, a fixed resistor value will result in a constant current passing through the heater. If the value of the resistor is changed, the resulting current will change accordingly.

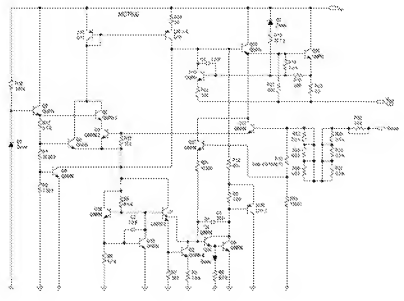

Figure 6

Figure 6 is a copy of a representative circuit diagram of the Motorola MC7805, found on page 2 of the Motorola data sheet of Appendix C. The resistor R of Figure 5 is connected the output pin Vout of the device, shown at the right of the circuit diagram, while all of the ground connections couple to a common node at the lower pin of the device, coupled, in the circuit of Figure 5, to the lower end of the resistor. One of ordinary skill will recognize that the current that passes through the resistor is only a small part of the total current that passes through the device, and only serves to fix the current value of the device.

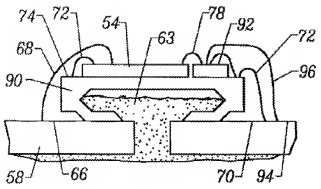

Figure 7.

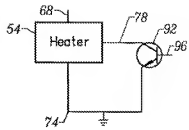

Figure 8.

Figures 7 and 8 are copies of Figures 6 and 7 of the Cozad '243 patent. Figure 7 shows the arrangement of the device, while Figure 8 provides a circuit diagram. In this embodiment, the load resistor is replaced with a load transistor 92. The heater 54 and load transistor 92 are shown in Figure 7 positioned on the boiler 90. The Cozad '243 patent describes the operation of the device, stating that "[t]he transistor is used as a load and a secondary heating source. The load transistor 92 allows dynamic output loading. The transistor 92 may be mounted onto the boiler 54, manufactured into the boiler 54, or mounted remotely."[12] It can be seen that, by changing a bias value of the transistor, the load can be changed, effectively permitting control of the current output of the device. Inasmuch as the heat produced by the heater 54 is a function of the current, the heat output can be controlled by the transistor 92.

Referring to the operation of the Cozad '243 patent's devices, it is well known that wherever electric current passes through a conductive material, heat is generated in proportion to the resistance of the material and the current passing therethrough. Resistors in an electrical circuit are used for many purposes, including impedance control, voltage biasing, and circuit loading, as in the present case. Heat generated in these and other circuit components is generally considered parasitic or undesirable, and in some circuits necessitates measures to cool the device to prevent damage to the circuit. The Cozad '243 patent, being directed to a heating device, places the load resistors in or on the boiler, thereby converting what would otherwise be waste heat into a secondary heat source. In the embodiment of Figures 6 and 7, where a transistor 92 is employed in place of a load resistor, the transistor is likewise positioned on the boiler.

[12] Cozad '243 patent, column 4, lines 46-49.

However, it is important to note that these measures, i.e., placing the load resistors or the transistor 92 on the boiler, are merely incremental economies that serve to prevent waste of heat that is an inevitable byproduct of the operation of the circuit. Clearly, the Cozad '243 patent does not consider the transistor 92 a primary heat source or as being capable of providing sufficient heat to operate independent of the heater. In particular, the transistor 92 is explicitly described as a secondary heat source.[13] One of ordinary skill will recognize that the transistor 92 of Figures 6 and 7 will produce a comparatively small proportion of the total heat generated, since the transistor is located in a control branch of the circuit, while most of the current entering the circuit at input 68 does not pass through the transistor.

Finally, the Cozad '243 patent makes clear that it is the heater 54 that is controlled to produce a predetermined temperature, and that operation and control of the transistor is primarily for the purpose of controlling the heater 54, not as an independent or primary heat source.[14] The transistor 92 of Cozad '243 is not required to generate any heat, much less reach a selected temperature; that is the role of the heater 54 which is present in all embodiments.

Rejections Under 35 U.S.C. § 102

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990).

The Examiner has rejected claims 1, 4, 5, and 16 under 35 U.S.C. § 102(b) as being anticipated by the Cozad '243 patent (U.S. 6,160,243).

Claim 1 recites, "at least one transistor formed in the semiconductor material and operable to generate heat above a selected threshold; [and] a fluid retaining chamber integral

[13] Cozad '243 patent, column 4, lines 45 and 46.

[14] See Cozad '243 patent, column 3, lines 54-57 and column 5, lines 5-7.

with the semiconductor material ...." The Cozad '243 patent fails to anticipate at least these limitations of claim 1. The term *generate heat*, as used in claim 1, refers to heat produced within the transistor, rather than heat produced by some outside element controlled by the transistor. This is clear from a review of the specification, which states, for example, "[t]he channel region [of the transistor] has a resistance ... to electric current so as to generate heat ... when conducting electric current,"[15] and "the channel resistance ... of the channel region generates the heat and transfers that heat to the chamber."[16] The specification also states,

> The heater 10 may be made easier and less expensively than known microchip heaters using ohmic resistors. Fewer mask processing steps are required and the expensive process control need to deposit and etch exotic resistor layers is eliminated. No expensive or exotic materials need be used. This results in simplified processing and less expense to fabricate the heater 10. Further, the cost is reduced since significant chip size reduction is achieved by the fact that the heater 10 does not require separate driving transistor and ohmic resistor assemblies be fabricated, both the driving transistor and the resistive element are combined together as the same element in the heater 10.

The Examiner has cited the transistor 92 shown in Figures 7 and 8 as being analogous to the transistor of claim 1. However, the Cozad '243 patent states that this transistor is provided instead of the load resistor, to allow "dynamic loading," and that as a heat source, the transistor is secondary to the resistive heater 54.[17] There is no teaching that this transistor is "operable to generate heat above a selected threshold," as recited in claim 1, nor would such a character be inherent.

The Examiner is basing his entire position on just 4 words in the entire Cozad '243 reference, quoted here in their context as follows: "The transistor 92 may be mounted onto the boiler 54, manufactured into the boiler 54, or mounted remotely."[18]

The four words, "manufactured into the boiler" is the total basis for this rejection. If Cozad '243 is read in its entirety and the circuit studied, it can be seen that only a small portion of the total current passes through the load transistor 92. The Cozad '243 patent teaches a

[15] Paragraph 30 of the '552 publication.

[16] Paragraph 34 of the '552 publication.

[17] Cozad '243 patent, column 4, lines 48-49.

[18] Cozad, column 4, lines 46-49

resistive, i.e., ohmic, heater,[19] and provides the transistor to control the heat produced, describing the transistor as a *secondary* heat source.

The transistor 92 of Cozad '243 does not generate heat above a selected threshold. It merely is positioned to avoid wasting the heat, but the transistor itself is does not, and cannot generate the heat needed for operation. It would be inappropriate, in the absence of a clear teaching, to interpret the Cozad '243 patent as providing a transistor "operable to generate heat above a selected threshold," as recited in claim 1. This is especially true in view of the fact that *every embodiment* of the Cozad '243 patent includes a resistive heater 54, while in the only embodiment that makes use of heat generated by a transistor, the transistor has a separate primary function, i.e., dynamic load.

The transistor 92 of Cozad '243 is not operated to produce heat, but rather to control the heater. This claimed feature is therefore missing from Cozad '243.

The term *formed*, as used in claim 1, has a clear and specific meaning when viewed in light of the specification. For example, the specification states, "A channel region 20 of the MOSFET is *formed* in the substrate 12 between the source and drain regions 14 and 16 to conduct electric current between the source and drain regions. The channel region 20 has a resistance ... to electric current so as to generate heat ... when conducting electric current."[20] As used in the claims and specification, *formed* is used to refer to processes employed in the production of semiconductor devices. Thus, a transistor formed in a semiconductor material is a transistor that is created using such processes, and would be readily understood as such by one of ordinary skill in the art. The Cozad '243 patent fails to anticipate this limitation, as well, but provides a confusing array of related terms, in reference to various features, including "formed within,"[21] "implanted,"[22] "positioned within,"[23] "manufactured into,"[24] and "internal,"[25], none of

[19] Cozad '243 patent, column 3, lines 54-57.

[20] Paragraph 30 of the '552 publication.

[21] Cozad '243 patent, column 3, line 48.

[22] Cozad '243 patent, column 3, line 50.

[23] Cozad '243 patent, column 4, line 14.

[24] Cozad '243 patent, column 4, line 49.

which is well defined. The passage cited by the Examiner indicates that the transistor 92 may be mounted onto the boiler 54, manufactured into the boiler 54, or mounted remotely. There is no teaching or explanation of what is meant by *manufactured into*.

Accordingly, the Cozad '243 patent fails to anticipate all the limitations of claim 1.

Clearly, claim 1 is allowable over the Cozad '243 patent, together with its dependent claims, including claims 4, 5, and 16.

Claims 5 and 16 are also allowable on their own merits. Claim 5 recites, "a dielectric layer extending over the semiconductor wall portion and facing toward the fluid chamber, being positioned between the semiconductor material and the chamber." The Cozad '243 patent fails to anticipate this limitation. The Examiner cites the Cozad '243 patent's boiler chamber 61,[26] formed in the boiler 52, and the insulating substrate 58 as being analogous, respectively, to the chamber formed in the semiconductor material and the dielectric layer of claim 5. However, a review of Figure 3, above, shows that the boiler 52, comprising the boiler chamber 61, is mounted on the insulating substrate 58. There is no point at which the insulating substrate 58 is positioned between the semiconductor material of the boiler 52 and the chamber. Clearly, the Cozad '243 patent does not anticipate claim 5, which is thus allowable.

Claim 16 recites, "a dielectric layer extending over a first face of the semiconductor material with the fluid to be heated positioned adjacent to the dielectric layer on a side thereof opposite the transistor." The Cozad '243 patent fails to anticipate this limitation. The Examiner rejects claim 16 on the same grounds as claim 5. However, in Figure 7 it can be seen that the boiler chamber 52 is not on a side of the insulating substrate 58 opposite the transistor 92, as would be necessary to anticipate claim 16, but is instead on the same side of the insulating substrate as the transistor. Accordingly, 16 is not anticipated by the Cozad '243 patent, but is allowable thereover.

The Examiner has indicated that he considers claim 1 to be generic.[27] While applicants agree with the Examiner that, if claim 1 is found to be allowable, the withdrawn claims will also

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[25] Cozad '243 patent, column 4, line 67.

[26] Misnumbered 60 in Figure 4 of Cozad '243.

[27] See Restriction Requirement of December 2, 2003.

be allowable, in particular independent claim 21 and its dependent claims, applicants note that claim 1 recites, in part, "a fluid to be heated positioned within the fluid retaining chamber ...." This limitation is not found in independent claim 21, and is not considered by the applicants to be an element thereof.

VIII. CLAIMS APPENDIX

1. (Previously Presented) An integrated heater comprising:

a semiconductor material;

at least one transistor formed in the semiconductor material and operable to generate heat above a selected threshold;

a fluid retaining chamber integral with the semiconductor material, the walls of the chamber being formed of the semiconductor material; and

a fluid to be heated positioned within the fluid retaining chamber and adjacent to the transistor to receive the heat generated by the transistor.

2. (Canceled)

3. (Canceled)

4. (Previously Presented) The integrated heater of claim 1 wherein the semiconductor material has a wall portion adjacent to the transistor to transmit heat generated by the transistor through the semiconductor wall portion, and further including a body having a wall portion positioned adjacent to and in sealing engagement with the semiconductor wall portion,

such that the semiconductor wall portion and the body wall portion together define the fluid chamber.

5. (Currently Amended) The integrated heater of claim 1 wherein the semiconductor material has a wall portion adjacent to the transistor and defining at least a portion of the chamber, the integrated heater further including a dielectric layer extending over the semiconductor wall portion and facing toward the fluid chamber, being positioned between the semiconductor material and the chamber.

6. (Withdrawn) The integrated heater of claim 1, further including a thermally insulating barrier formed in the semiconductor material extending about the transistor to limit transmission in the semiconductor material of the heat generated by the transistor beyond the insulating barrier.

7. (Withdrawn) The integrated heater of claim 1 wherein the semiconductor material extends laterally beyond the transistor to provide a lateral semiconductor portion, and the fluid to be heated is positioned laterally adjacent to the transistor and adjacent to the lateral semiconductor portion to receive the heat generated by the transistor which is transmitted laterally to the lateral semiconductor portion.

8. (Withdrawn) The integrated heater of claim 7, further including a dielectric layer extending over the semiconductor material with a window formed in a portion of the dielectric layer at a location adjacent to the lateral semiconductor portion, and wherein the

fluid to be heated is positioned at the window to receive the heat generated by the transistor which passes through the window.

9. (Canceled)

10. (Withdrawn) The integrated heater of claim 7 wherein the lateral semiconductor portion has a wall portion to transmit heat to the object to be heated that is generated by the transistor and transmitted through the lateral semiconductor portion, and further including a body having a wall portion positioned adjacent to and in sealing engagement with the lateral semiconductor wall portion, such that the lateral semiconductor wall portion and the body wall portion together define the fluid chamber.

11. (Withdrawn) The integrated heater of claim 7, further including a thermally insulating barrier formed in the semiconductor material extending laterally outward of and about the transistor and the lateral semiconductor portion to limit transmission in the semiconductor material of the heat generated by the transistor laterally beyond the insulating barrier.

12. (Withdrawn) The integrated heater of claim 7, further including has a dielectric layer extending over a first face of the semiconductor material and a window formed in a portion of the dielectric layer over the lateral semiconductor portion, with the object to be heated positioned at the window to receive the heat generated by the transistor which passes through the window, and further including a thermally insulating barrier formed in the semiconductor material extending laterally outward of and about the transistor and the window

to limit transmission in the semiconductor material of the heat generated by the transistor laterally beyond the insulating barrier.

13. (Withdrawn) The integrated heater of claim 12, further including a thermally insulating layer extending over a second face of the semiconductor material opposite the first face, and the insulating barrier is positioned between the dielectric layer and the insulating layer.

14. (Withdrawn) The integrated heater of claim 12 wherein the object to be heated is a fluid chamber.

15. (Withdrawn) The integrated heater of claim 12, further including a body having a wall portion positioned adjacent to and in sealing engagement with the dielectric layer about the window, such that the body wall portion defines a fluid chamber as the object to be heated with the heat being supplied thereto through the window.

16. (Previously Presented) The integrated heater of claim 1, further including a dielectric layer extending over a first face of the semiconductor material with the fluid to be heated positioned adjacent to the dielectric layer on a side thereof opposite the transistor to receive the heat generated by the transistor.

17. (Withdrawn) The integrated heater of claim 16, further including a thermally insulating barrier formed in the semiconductor material to define a portion of the semiconductor material inward to the insulating barrier positioned to receive the heat generated

by the transistor, the insulating barrier being of a material which limits transmission of the heat generated by the transistor and received by the inward portion of the semiconductor material beyond the insulating barrier.

18. (Withdrawn) The integrated heater of claim 16, further including a thermally insulating layer extending over a second face of the semiconductor material opposite the first face.

19. (Withdrawn) The integrated heater of claim 16, further including a body having a wall portion positioned adjacent to and in sealing engagement with the dielectric layer, such that the dielectric layer and the body wall portion together define a fluid chamber as the object to be heated.

20. (Canceled)

21. (Withdrawn) An integrated heater comprising:

a semiconductor material;

a plurality of heat producing transistors formed in the semiconductor material and selectively operable to generate heat above a selected threshold; and

a heat receiving chamber for containing a fluid to be heated, the heat receiving chamber being formed integrally with the semiconductor material.

22. (Withdrawn) The integrated heater of claim 21 wherein the heat receiving chamber is a fluid holding chamber coupled to and positioned adjacent to the semiconductor material.

23. (Withdrawn) The integrated heater of claim 21, further including a thermally insulating barrier formed in the semiconductor material extending a perimeter about the transistors to limit transmission of the heat generated by the transistors beyond the insulating barrier.

24. (Original) An integrated heater comprising:

a semiconductor substrate;

a source region disposed in the semiconductor substrate;

a drain region disposed in the semiconductor substrate;

a channel region disposed in the semiconductor substrate between the source and drain regions to conduct electric current between the source and drain regions, the channel region having a resistance when conducting current to generate heat above a selected threshold;

a dielectric layer disposed on the channel region;

a gate electrode disposed on the dielectric layer to control the current conducted by the channel region; and

an object to be heated positioned to receive the heat generated by the resistance of the channel region.

25. (Original) The integrated heater of claim 24 wherein the object to be heated is a fluid chamber positioned adjacent to the semiconductor material.

26. (Original) The integrated heater of claim 24 wherein the object to be heated is a fluid chamber formed in the semiconductor substrate.

27. (Withdrawn) The integrated heater of claim 24, further including a thermally insulating barrier formed in the semiconductor substrate and extending at least partially about the channel region to define a portion of the semiconductor substrate inward to the insulating barrier positioned to receive the heat generated by the resistance of the channel region.

28. (Previously Presented) The integrated heater of claim 24 wherein the semiconductor substrate has a wall portion integrally formed with and adjacent to the channel region to transmit the heat generated by the resistance of the channel region through the semiconductor wall portion, and further including a body having a wall portion positioned adjacent to the semiconductor wall portion and defining a fluid chamber as the object to be heated.

29. (Original) The integrated heater of claim 28, further including a heat transmitting dielectric layer positioned between the semiconductor wall portion and the body wall portion.

30. (Original) The integrated heater of claim 24, further including a body having a wall portion positioned adjacent to the dielectric layer and defining a fluid chamber as the object to be heated.

31. (Withdrawn) The integrated heater of claim 24, further including a thermally insulating layer positioned toward a side of the semiconductor substrate away from the dielectric layer.

32. (Withdrawn) The integrated heater of claim 31, further including a thermally insulating barrier formed in the semiconductor substrate to define an inward portion of the semiconductor substrate inward of the insulating barrier and positioned to receive the heat generated by the resistance of the channel region, the insulating barrier being of a material which limits transmission of the heat generated by the resistance of the channel region and received by the inward portion of the semiconductor material beyond the insulating barrier, the object to be heated being in thermal communication with the inward portion of the semiconductor material.

33. (Withdrawn) The integrated heater of claim 32 wherein the insulating barrier projects substantially fully between the dielectric layer and the insulating layer.

34. (Original) The integrated heater of claim 24, further including an overlay dielectric layer overlaying the gate electrode, the object to be heated being positioned adjacent to the overlay dielectric layer.

35. (Original) The integrated heater of claim 34, further including a body having a wall portion positioned adjacent to the overlay dielectric layer, across from the gate electrode, and defining a fluid chamber as the object to be heated.

36. (Withdrawn) The integrated heater of claim 35, further including a thermally insulating barrier formed in the semiconductor substrate and extending at least partially about the channel region to define a portion of the semiconductor substrate inward of the insulating barrier and adjacent to the fluid chamber such that the inward portion of the semiconductor substrate is in thermal communication with the fluid chamber.

37. (Withdrawn) The integrated heater of claim 36, further including a thermally insulating layer positioned toward a side of the semiconductor substrate away from the dielectric layer.

38. (Withdrawn) The integrated heater of claim 37 wherein the insulating barrier projects substantially fully between the dielectric layer and the insulating layer.

39. (Withdrawn) The integrated heater of claim 24 wherein the semiconductor substrate extends laterally beyond the source and drain regions to provide a lateral semiconductor substrate portion, and the object to be heated is positioned adjacent to the lateral semiconductor substrate portion to receive the heat generated by the resistance of the channel region which is transmitted laterally thereto through the lateral semiconductor substrate portion.

40. (Withdrawn) The integrated heater of claim 39, wherein the dielectric layer extends laterally over the lateral semiconductor substrate portion, and further including an overlay dielectric layer overlaying the gate electrode and a window formed in of the overlay dielectric layer at a location corresponding to the lateral semiconductor substrate portion, and

wherein the object to be heated is positioned at the window to receive the heat transmitted laterally through the lateral semiconductor substrate portion generated by the resistance of the channel region and which passes through the window.

41. (Withdrawn) The integrated heater of claim 40, further including a body having a wall portion positioned adjacent to the window and defining a fluid chamber as the object to be heated with the heat being supplied thereto through the window.

42. (Original) The integrated heater of claim 24 wherein the gate electrode is metal.

43. (Original) The integrated heater of claim 24 wherein the object to be heated is a fluid.

44. (Previously Presented) An integrated heater circuit comprising:

a semiconductor substrate;

a source region disposed in the semiconductor substrate;

a drain region disposed in the semiconductor substrate;

a channel region disposed in the semiconductor substrate between the source and drain regions to conduct electric current between the source and drain regions, the source, drain and channel regions producing heat when conducting current to generate heat above a selected threshold;

a dielectric layer disposed on the channel region;

a gate electrode disposed on the dielectric layer to control the current conducted by the channel region; and

a chamber to be heated formed integral with the semiconductor substrate to receive the heat generated by the integrated heater circuit.

45. (Previously Presented) The integrated heater of claim 44 wherein the heat receiving chamber is a fluid holding chamber that includes the semiconductor material.

46. (Previously Presented) The integrated heater of claim 44 further including:

an electrically insulating layer positioned between the semiconductor material and the chamber.

47. (Previously Presented) The integrated heater circuit of claim 44 wherein the chamber walls are composed of semiconductor material.

48. (Previously Presented) The integrated heater circuit of claim 47 further including:

a layer of electrically insulating material positioned between the chamber walls and the chamber.

49. (Previously Presented) The integrated heater circuit of claim 44 wherein the chamber walls are composed of an integrated layer other than the semiconductor layer.

IX. EVIDENCE APPENDIX

Appendix A is a copy of the published application under consideration.

Appendix B is a copy of the Cozad '243 patent, U.S. patent No. 6,160,243, relied upon by the Examiner in rejecting claims 1, 5, 6, and 16.

Appendix C is a copy of the Motorola MC7800/D datasheet, which includes the specifications of the Motorola 7805 cited in the Cozad '243 patent.

Appendix A

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(54) **HEATING ELEMENT FOR MICROFLUIDIC AND MICROMECHANICAL APPLICATIONS**

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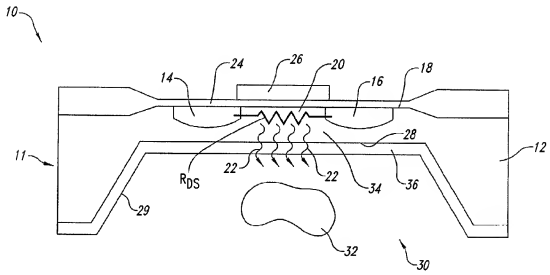
(52) **U.S. Cl.** **219/209**; 392/407

(57) **ABSTRACT**

An integrated heater formed as a field effect transistor in a semiconductor substrate, with the transistor having source and drain regions with a channel region extending therebetween to conduct current. The channel region has a resistance when conducting current to generate heat above a selected threshold. A dielectric layer is disposed on the channel region and a gate electrode is disposed on the dielectric layer to control the current of the channel region. A thermally insulating barrier may be formed in the semiconductor material extending about the transistor. The object to be heated is positioned to receive the heat generated by the resistance of the channel region; the object may be a fluid chamber.



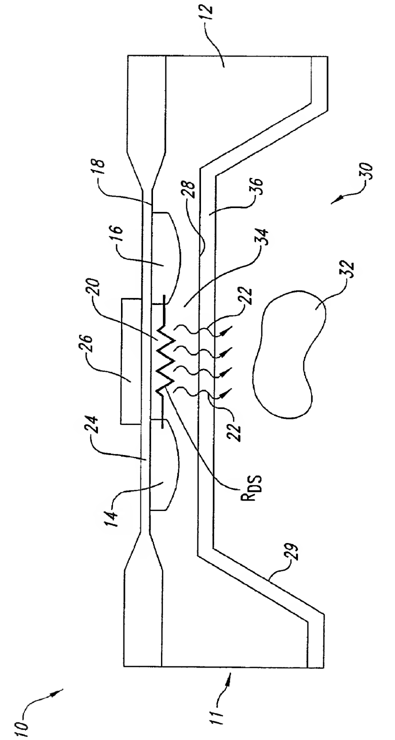


Fig. 1

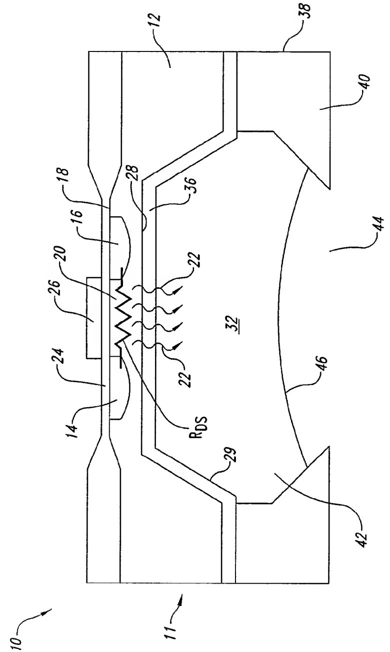


Fig. 2

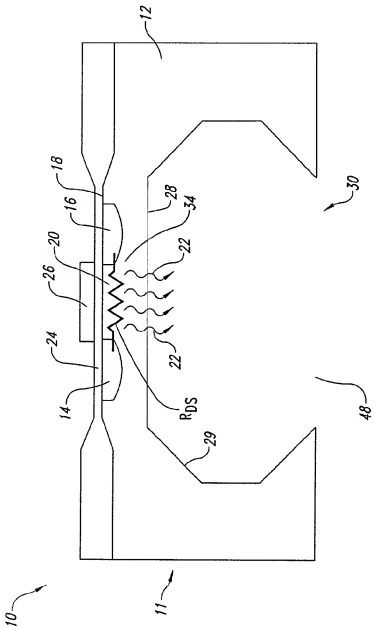


Fig. 3

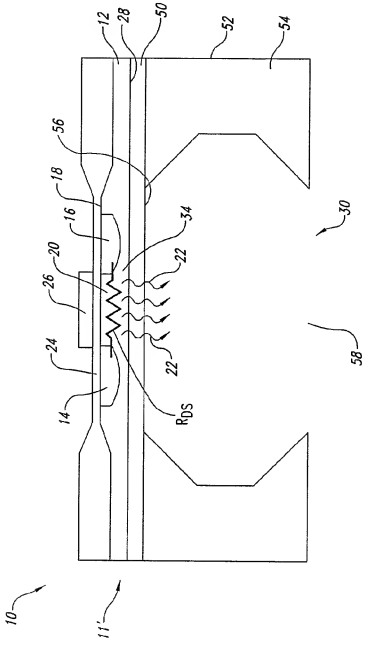


Fig. 4

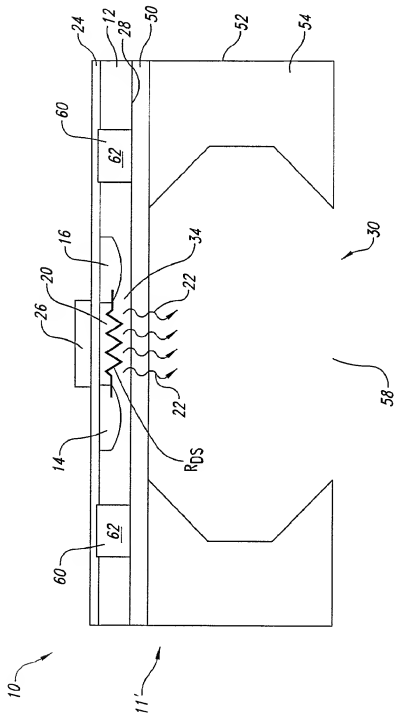


Fig. 5

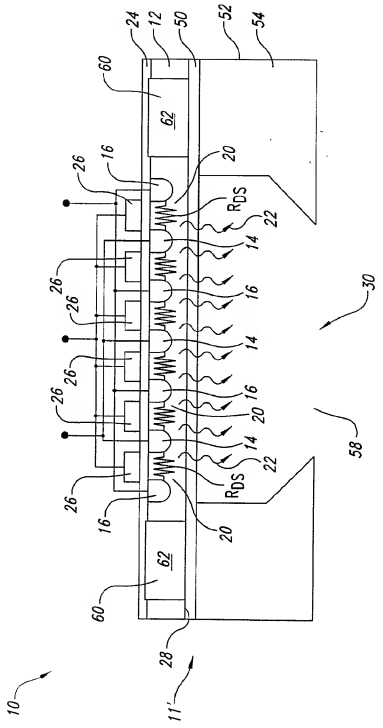


Fig. 6

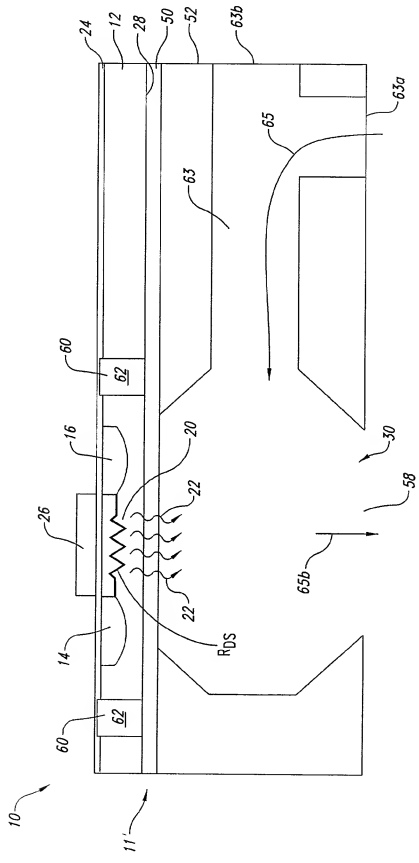


Fig. 7

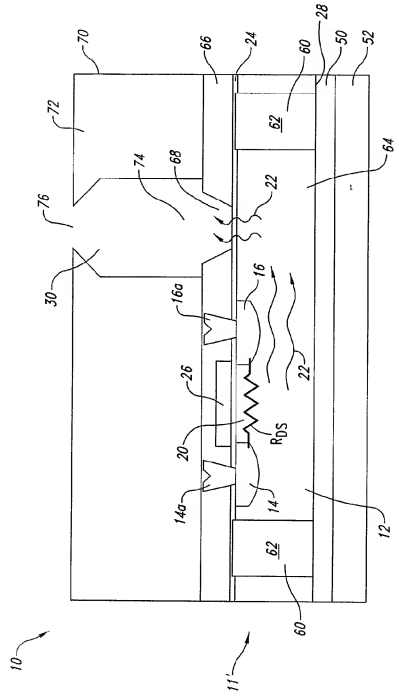


Fig. 8

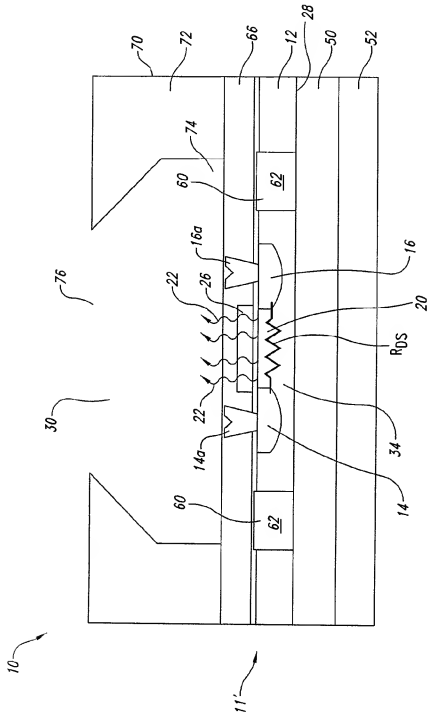


Fig. 9

HEATING ELEMENT FOR MICROFLUIDIC AND MICROMECHANICAL APPLICATIONS

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to microchip heaters for microfluidic and micromechanical applications, such as integrated chemical microreactors for decomposition and detection of bioorganic compounds such as DNA, ink-jet printer heaters for firing ink for printing purposes, optical switching based on vapor bubble formation to deflect a light beam, and optical switching based on liquid crystals.

[0003] 2. Description of the Related Art

[0004] As is known, some fluids are processed at temperatures that should be regulated in an increasingly more accurate way, for example, when chemical or biochemical reactions are involved. In such situations, there is often also a need to use very small quantities of fluid, owing to the cost of the fluid, or to low availability.

[0005] This is the case, for example, of the DNA amplification process (PCR, i.e., Polymerase Chain Reaction process), wherein accurate temperature control in the various steps (repeated predetermined thermal cycles are carried out), the need to avoid as far as possible thermal gradients where fluids react (to obtain here a uniform temperature), and also reduction of the used fluid (which is very costly), are of importance in obtaining good reaction efficiency, or even to make reaction successful. Microchip heaters are particularly suited for this application.

[0006] Other examples of fluid processing with the above-described characteristics are associated for example with implementation of chemical and/or pharmacological analyses, and biological examinations. Other situations that require a miniaturized heater that is one or more of more accurate, quicker reacting, more durable, longer-lived, more controllable and less expensive to manufacture include ink-jet printers heaters and optical switching heaters to name a few.

[0007] At present, various techniques allow thermal control of chemical or biochemical reagents. In particular, from the end of the 1980s, miniaturized devices were developed, and thus had a reduced thermal mass, which could reduce the times necessary to complete the DNA amplification process. Recently, monolithic integrated devices of semiconductor material have been proposed, able to process small fluid quantities with a controlled reaction, and at a low cost (see, for example, U.S. patent application Ser. Nos. 09/779,980, filed on Feb. 8, 2001; 09/874,382 filed on Jun. 4, 2001; and 09/965,128, filed Sep. 26, 2001; all assigned to STMicroelectronics, S.r.l. and incorporated herein by reference).

[0008] These devices comprise a semiconductor material body accommodating buried channels that are connected, via an input trench and an output trench, to an input reservoir and an output reservoir, respectively, to which the fluid to be processed is supplied, and from which the fluid is collected at the end of the reaction. Above the buried channels, heating elements and thermal sensors are provided to control the thermal conditions of the reaction (which generally requires different temperature cycles, with accurate control of the latter), and, in the output reservoir, detection electrodes are provided for examining the reacted fluid. The heat is generated by supplying electric current to a metal heating element formed on a wafer comprising a semiconductor body with contact regions in electrical contact with the two opposite ends of the heating element and connected to a drive transistor, typically a MOSFET formed on the same wafer.

[0009] Current inkjet technology relies on placing a small amount of ink within an ink chamber, rapidly heating the ink and ejecting it to provide an ink drop at a selected location on an adjacent surface, such as a sheet of paper. Traditionally, ohmic resistors which heat up rapidly when current is passed therethrough have been used to provide the necessary temperature increase of the ink. See, for example, a detailed discussion of ink ejection in an article titled "Thermodynamics and Hydrodynamics of Thermal Ink Jets," by Allen et al., *Hewlett-Packard Journal*, May 1985, pp. 20-27, incorporated herein by reference.

[0010] Microchips are highly suited for miniaturized heater applications. Generally, present techniques for generating local heating in a microchip are based on ohmic resistors made of metal alloys, such as TaAl, HfB, ternary alloys, etc., or polycrystalline semiconductors. The heating resistor is driven by external circuitry or an integrated power MOSFET. In existing applications, such as thermal ink-jet printers, the heating resistor value is preferably higher than the MOSFET channel resistance (R_{ON} or R_{DS}) to minimize the parasitic effects and dissipate power in the heating resistor only. Normally, each power MOSFET occupies a large percentage of the chip area to minimize its R_{ON}.

[0011] One drawback with this arrangement is that the resistance of such ohmic resistors is fixed and cannot be modulated, thus limiting their flexibility. Other drawbacks are that ohmic resistors are subject to material degradation (such as oxidation, segregation, etc.), and electromigration, especially at high temperatures. These phenomena limit their lifetime and are a concern for the reliability of devices that incorporate them into their design.

[0012] Yet another drawback is power control. Ohmic resistors, which are either current or voltage driven, dissipate a power that is a quadratic function of the parameters. This results in poor control over their output, as small variations in current or voltage can cause significant fluctuations in power and temperature output.

[0013] The present invention provides a miniaturized heater that provides the desired characteristics for many microfluidic and micromechanical applications, while overcoming the drawbacks noted above, while providing other related advantages.

BRIEF SUMMARY OF THE INVENTION

[0014] The present invention resides in an integrated heater comprised of a semiconductor material, with at least one transistor formed in the semiconductor material and operable to generate heat, and an object to be heated positioned adjacent to the transistor to receive the heat generated by the transistor. In one embodiment disclosed, the object to be heated is a fluid chamber positioned adjacent to the semiconductor material. The object to be heated may be, but is not limited to, a fluid chamber formed in the semiconductor material.

[0015] In some disclosed embodiments, the semiconductor material has a wall portion adjacent to the transistor to transmit heat generated by the transistor through the semiconductor wall portion. The heater further includes a body having wall portion positioned adjacent to and in sealing engagement with the semiconductor wall portion, such that the semiconductor wall portion and the body wall portion together define a fluid chamber as the object to be heated. The object to be heated may take forms other than a fluid chamber.

[0016] In some disclosed embodiments, the integrated heater further includes a thermally insulating barrier formed in the semiconductor material extending about the transistor to limit transmission in the semiconductor material of the heat generated by the transistor beyond the insulating barrier.

[0017] The heater may be manufactured with the semiconductor material extending laterally beyond the transistor to provide a lateral semiconductor portion, and the object to be heated may be positioned laterally adjacent to the transistor and adjacent to the lateral semiconductor portion to receive the heat generated by the transistor that is transmitted laterally to the lateral semiconductor portion. In at least one such embodiment, the heater has a dielectric layer extending over the semiconductor material with a window formed in a portion of the dielectric layer at a location adjacent to the lateral semiconductor portion, with the object to be heated positioned at the window to receive the heat generated by the transistor which passes through the window. The lateral semiconductor portion may have a wall portion to transmit heat to the object to be heated that is generated by the transistor and transmitted through the lateral semiconductor portion, and the heater may include a body with a wall portion positioned adjacent to and in sealing engagement with the lateral semiconductor wall portion, such that the lateral semiconductor wall portion and the body wall portion together define a fluid chamber as the object to be heated. In this embodiment, the thermally insulating barrier formed in the semiconductor material extends laterally outward of and about the transistor and the lateral semiconductor portion.

[0018] The integrated heater may be manufactured using a plurality of transistors formed in the semiconductor material and selectively operable to generate heat.

[0019] The integrated heater may be manufactured as a field effect transistor formed in a semiconductor substrate, with the transistor having a source region, a drain region and a channel region between the source and drain regions to conduct electric current, with the channel region having a resistance when conducting current to generate heat above a selected threshold. A dielectric layer is disposed on the channel region. A gate electrode is disposed on the dielectric layer to control the current conducted by the channel region. The object to be heated is positioned to receive the heat generated by the resistance of the channel region.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S)

[0020] In order to assist understanding of the present invention, preferred embodiments are now described, purely by way of non-limiting example, with reference to the attached drawings, wherein:

[0021] **FIG. 1** is a side elevational, cross-sectional schematic drawing of a MOSFET heater according to the invention;

[0022] **FIG. 2** is a side elevational, cross-sectional schematic drawing of a first alternative embodiment of the MOSFET heater of **FIG. 1** with a fluid chamber;

[0023] **FIG. 3** is a side elevational, cross-sectional schematic drawing of a second alternative embodiment of the MOSFET heater of **FIG. 1** with a fluid chamber formed fully in the semiconductor material;

[0024] **FIG. 4** is a side elevational, cross-sectional schematic drawing of a third alternative embodiment of the MOSFET heater of **FIG. 1** with a fluid chamber;

[0025] **FIG. 5** is a side elevational, cross-sectional schematic drawing of a fourth alternative embodiment of the MOSFET heater of **FIG. 1** with a fluid chamber and a thermally insulating trench extending about the MOSFET;

[0026] **FIG. 6** is a side elevational, cross-sectional schematic drawing of a fifth alternative embodiment of the MOSFET heater of **FIG. 1** with a fluid chamber using a multiple source/drain MOSFET and a thermally insulating trench extending about the MOSFET;

[0027] **FIG. 7** is a side elevational, cross-sectional schematic drawing of a sixth alternative embodiment of the MOSFET heater of **FIG. 1** with a fluid chamber fed by a channel and a thermally insulating trench extending about the MOSFET;

[0028] **FIG. 8** is a side elevational, cross-sectional schematic drawing of a seventh alternative embodiment of the MOSFET heater of **FIG. 1** with a fluid chamber formed laterally offset from the MOSFET and on a front side of the MOSFET; and

[0029] **FIG. 9** is a side elevational, cross-sectional schematic drawing of an eighth alternative embodiment of the MOSFET heater of **FIG. 1** with a fluid chamber formed on a front side of the MOSFET immediately thereover and a thermally insulating trench extending about the MOSFET.

DETAILED DESCRIPTION OF THE INVENTION

[0030] As shown in the drawings for purposes of illustration, the present invention is embodied in an integrated heater, indicated generally by reference numeral **10**, formed on a wafer **11**. As shown in **FIG. 1**, the wafer **11** has a substrate **12** of monocrystalline semiconductor material, for example silicon. The substrate **12** has been processed using well-known MOSFET manufacturing techniques to form a source region **14** and a drain region **16** of a MOSFET in the substrate toward an upper side or surface **18** thereof. A channel region **20** of the MOSFET is formed in the substrate **12** between the source and drain regions **14** and **16** to conduct electric current between the source and drain regions. The channel region **20** has a resistance R_{ON} or R_{DS}, indicated schematically by resistor symbol, to electric current so as to generate heat, indicated by arrows **22**, when conducting electric current.

[0031] A dielectric layer **24**, for example an oxide, is formed on the upper side of the substrate **12** and extends across the channel region **20**. A gate electrode **26** of the

MOSFET is formed on the dielectric layer **24** above the channel region **20** to control the current conducted by the channel region. The gate electrode can be composed of any acceptable material, such as polysilicon, a polysilicon with a silicide layer thereon, or metal or any other conductive layer that is compatible with the process of the present invention. A metal silicide on top of a polysilicon is preferred in many instances because such a gate has a very low electrical resistivity with the advantage of a metal top layer for good thermal conductivity. The process technology and steps for forming such are well known. The MOSFET can be of any suitable type, such as LDMOS, VDMOS, etc.

[0032] A lower side or surface **28** of the substrate **12** has a portion thereof below the channel region **20** (at the back of the wafer **11**) etched away or otherwise removed to reduce the thickness of the substrate in this area and to form a recess **29** in the substrate. The recess **29** defines at least in part forms a chamber **30** and serves as the object to be heated by the heat **22** generated by the channel region **20**. The chamber **30** may be sized and shaped to receive a substance **32** to which the heat **22** transmitted into the chamber **30** is transferred. The chamber **30** is positioned close to the channel region **20** to receive the heat **22** generated by the channel resistance R_{DS} when the channel region is conducting electric current. The substrate **12** is removed when forming the chamber **30** so as to leave only a thin wall portion **34** thereof remaining below the channel region **20** in order to have the heat source (i.e., the channel region) close to the substance **32** to be heated.

[0033] The lower side **28** of the substrate **12** has dielectric layer **36** formed thereon, such as by deposition or by being grown thereon. The dielectric layer **36** lines the portion of the lower side of the substrate that forms a part of the chamber **30**. If the substance **32** to be received in the chamber **30** for heating is a fluid, the dielectric layer **36** may be selected as a material that provides protection to the substrate **12** against any harmful effects the fluid may have on the substrate if direct contact occurred. In the case of a fluid, the fluid in the chamber **30** can come into direct contact with the chamber walls and such is desirable to get the fluid close to the channel region **20** to have improved transfer of heat to the fluid. The heat **22** is transmitted through the dielectric layer **36** to the chamber **30** so the dielectric layer is selected with thermal properties sufficient to transfer the desired amount of heat. The heater **10** may be used to heat substances other than fluids, in which case the lower side **28** of the substrate **12** may be used as a heat transfer surface and shaped as appropriate to contact the object to be heated, whether it be a flat object or a contoured object, with or without an intervening protective or other layer or other material.

[0034] As noted, the channel resistance R_{DS} (i.e., source-to-drain resistance) of the channel region **20** generates the heat **22** and transfers that heat to the chamber **30** where the substance **32** is at least temporarily located so as to be heated. The channel region **20** generates the heat **22** when a sufficient voltage is applied to the gate electrode **26** to cause conduction in the channel region **20** between the source and drain regions **14** and **16**, in a manner conventional with MOSFETs. The amount of heat **22** generated in a particular application can be controlled by the amount of voltage applied to the gate electrode **26** since the channel resistance R_{DS} in a MOSFET is a function of the gate voltage applied. A power MOSFET transistor can be used to achieve higher current conduction and an increased heating rating.

[0035] The channel resistance R_{DS} of the channel region **20** can be easily selected during fabrication of the MOSFET to produce a particular resistance value desired for a specific application, such as by varying the length and/or width of the channel region, the silicon doping used and/or the design layout so that the desired power is dissipated through the channel resistance R_{DS} when the MOSFET is on. It is noted that more normally doping of the channel region **20** is done in normal MOSFET production for the purpose of reducing the channel resistance, however, when the MOSFET is used as a heater, the doping is conducted to enhance/increase the resistance of the channel. A particular channel resistance R_{DS} is selected such that when the channel region **20** is conducting electric current, heat above a selected threshold is generated and transferred to the chamber **30** to heat the substance **32** in the chamber. The threshold is selected to supply the amount of heat desired to be transferred to the object to be heated or necessary to raise the temperature of the object to be heated or a substance to at least a desired temperature.

[0036] The MOSFET used in the heater **10** may be fabricated using conventional techniques to produce a channel resistance R_{DS} that may be from a few ohms to thousands of ohms, thus providing design flexibility. The operating temperature range of the channel resistance R_{DS} of the MOSFET can be between a few Celsius degrees and more than 1,000 Celsius degrees, thus providing sufficient heat for many microfluidic and micromechanical applications where local thermal gradients are required, such as to induce chemical reactions, or to produce mass and heat transportation such as to eject fluids or generate vapors. The substance **32** to which the heat **22** transmitted into the chamber **30** is transferred may be a fluid such as, but not limited to, ink, mixtures of organic materials, fluids for optical switching, and gases for environmental testing and medical applications, and the fluids mentioned in the Description of the Related Arts set forth herein, to name a few.

[0037] The heater **10** may be made easier and less expensively than known microchip heaters using ohmic resistors. Fewer mask processing steps are required and the expensive process control need to deposit and etch exotic resistor layers is eliminated. No expensive or exotic materials need be used. This results in simplified processing and less expense to fabricate the heater **10**. Further, the cost is reduced since significant chip size reduction is achieved by the fact that the heater **10** does not require separate driving transistor and ohmic resistor assemblies be fabricated, both the driving transistor and the resistive element are combined together as the same element in the heater **10**.

[0038] Increased reliability of performance for many applications will also be achieved using the heater **10**. The resistors currently used for inkjet and optical switching applications have limited lifetime and fail for electromigration or physical damage (such as from cavitation) after a few billions of cycles. The lifetime of the channel region **20** of the heater **10** functioning to provide the channel resistance R_{DS} that produces the heat **22** should last for several years of operating conditions, which for inkjet printer applications is longer than the life of the printer. This is because the channel resistance R_{DS} is made from durable silicon crystal.

This should allow the manufacture of inkjet printheads that are cheap and permanent, and do not need replacement during the normal lifetime of the inkjet printer.

[0039] The performance will also be increased for many applications when using the heater **10**. This is in part due to the drastic reduction of parasitic resistance that is associated with the prior art microchip heaters using ohmic resistors. In the past when using prior art microchip heaters using ohmic resistors, the channel resistance of the driving MOSFET was a main contributor to the parasitic resistance realized, in addition to the parasitic resistance of the metal traces that drive the transistor. With the heater **10**, the "parasitic resistance" of the MOSFET becomes the heating element and parasitic effects are now primarily the low resistance metal traces that drive the MOSFET of the heater.

[0040] Another performance increase is achieved because the MOSFET transistor used in the heater **10** can be drawn as small as a few squared microns, thus allowing packing of a huge number of transistors on the same chip. For inkjet printers applications, this means that printheads can be manufactured which are capable of printing very high resolution pictures in one single pass.

[0041] Yet another performance increase results from the fact that a power MOSFET can be designed in such a way that at operational current/voltage, any fluctuation in these parameters has an insignificant impact on the dissipated power. Thus, the heater **10** is of particular interest for microreactor applications, such as chips for biological analysis, where lower temperatures and good temperature control are needed.

[0042] A first alternative embodiment of the heater **10** is shown in **FIG. 2**. The heater **10** of **FIG. 2** has the same basic construction as the heater of **FIG. 1** except that the chamber **30** is in part formed by a body **38** that has a wall portion **40** that extends about the recess **29** in the substrate **12** on the back of the wafer **11**. The wall portion **40** of the body **38** is positioned adjacent to and in sealing engagement with the substrate **12** at its lower side **28**, with the dielectric layer **36** positioned therebetween. The wall portion **40** defines an open interior portion **42** that mates with the recess **29** to form the chamber **30**, and defines an orifice **44** through which the substance **32** can pass, which in **FIG. 2** is shown as a fluid with a meniscus **46**.

[0043] A second alternative embodiment of the heater **10** is shown in **FIG. 3**. The heater **10** of **FIG. 3** has the same basic construction as the heater of **FIGS. 1 and 2** except that the recess **29** formed in the substrate **12** on the back of the wafer **11** is shaped to form the entire chamber **30**, including an orifice **48**. If appropriate, the chamber **30** can be lined with a protective layer.

[0044] A third alternative embodiment of the heater **10** is shown in **FIG. 4**. The heater **10** of **FIG. 4** has a different construction than the heaters of FIGS. 1-3 in that the MOSFET is made on a SOI (silicon on insulator) wafer **11'** with the substrate **12** (such as silicon) having its lower side **28** engaging an oxide layer **50**. The heat **22** generated by the channel region **20** is transmitted through the oxide layer **50** to the chamber **30** so the oxide layer **50** is selected with thermal properties sufficient to transfer the desired amount of heat to the chamber. The structure of **FIG. 4** can be obtained by using two separate wafers, one for the heating device and one for the chamber **30**. The substrate for the chamber **30** can be any acceptable material for the chamber, including silicon, an organic polymer, sapphire, or any other suitable material. A layer **50** of an insulator is grown thereon that the back side of the wafer **12** is removed to a desired level and the wafer **11'** is connected to the substrate **12**. There are many acceptable techniques for doing this, one of which is described in pending application 854063.663, incorporated herein by reference.

[0045] In this third alternative embodiment, a body **52** made of silicon with a wall portion **54** defines the chamber **30** in conjunction with a lower side **56** of the oxide layer **50**. The wall portion **54** of the body **52** is positioned adjacent to and in sealing engagement with the lower side **56** of the oxide layer **50**. The wall portion **54** defines an orifice **58** through which the substance **32** can pass (not shown in **FIG. 4**).

[0046] A fourth alternative embodiment of the heater **10** is shown in **FIG. 5**. The heater **10** of **FIG. 5** has the same basic construction as the heater of **FIG. 4**, using the SOI wafer **11'** approach, except that a trench **60** is formed in the substrate **12** which is located laterally outward of and extends fully about the source and drain regions **14** and **16** and channel region **20**. The trench **60** may be left empty or filled with an insulating material **62** such as silicon oxide. The trench **60** serves as a thermally insulating barrier to limit the lateral transfer of the heat **22** generated by the channel region **20** in the substrate **12**, and as will be described below in greater detail, tends to contain the heat generated by the channel region and allow it to be better route the heat to the object to be heated. The trench **60** also serves to electrically isolate the MOSFET. The trench **60** projects fully between the dielectric layer **24** and the oxide layer **50**.

[0047] A fifth alternative embodiment of the heater **10** is shown in **FIG. 6**. The heater **10** of **FIG. 6** has the same basic SOI construction as the heater of **FIG. 5** except that it uses a multiple finger, power MOSFET with multiple source regions **14** electrically connected together, multiple drain regions **16** electrically connected together, and multiple gate electrodes **26** electrically connected together. There are, of course, multiple channel regions **20** between the adjacent source and drain regions. The trench **60** is located laterally outward of and extends fully about all of the source and drain regions **14** and **16** and channel regions **20** for the power MOSFET.

[0048] A sixth alternative embodiment of the heater **10** is shown in **FIG. 7**. The heater **10** of **FIG. 7** has the same basic SOI construction as the heater of **FIG. 5** except that the substrate **12** and the body **52** extend laterally beyond the source and drain regions **14** and **16**, the gate electrode **26** and the channel region **20**, and a fluid channel **63** is provided in the body **52** which extends between a channel entrance aperture **63*a*** and the chamber **30**. A fluid flow, shown by arrow **65*a***, may enter the entrance aperture **63*a*** and flow to the chamber **30** whereat the heat **22** generated by the channel region **20** is transferred to the fluid. The heated fluid can then exit the chamber **30** through the orifice **58**, shown by arrow **65*b***. If the heater **10** is used as an inkjet printhead, the exiting heated fluid ink can be sprayed onto the paper or other material to be printed. The fluid channel **63** may also have an additional entrance aperture **63*b*** in fluid communication with the channels of neighboring heaters, if desired.

[0049] A seventh alternative embodiment of the heater **10** is shown in **FIG. 8**. The heater **10** of **FIG. 8** uses the same basic SOI construction; however, there is no chamber formed by the silicon body **52**, which is a slab in this embodiment. Further, the chamber **30** is not located directly below the channel region **20** to receive the heat **22** generated thereby. Instead, the chamber **30** is located on the front of the wafer **11**' and is laterally offset from the MOSFET, as will be described below.

[0050] In particular, the substrate **12** has a lateral portion **64** that extends laterally beyond the source and drain regions **14** and **16**, the gate electrode **26** and the channel region **20**. The heat **22** generated by the channel region **20** is transmitted laterally to the lateral substrate portion **64**. In this seventh alternative embodiment, the oxide layer **50** is selected with thermal insulating properties and thickness to limit the amount of the heat **22** generated by the channel region **20** that is transferred through the oxide layer **50**, i.e., the oxide layer **50** serves as a thermal barrier. The insulating oxide layer **50**, in conjunction with the trench **60**, serve as thermally insulating barriers to limit the transmission of the heat **22** generated by the channel region **20** other than in the lateral direction to the lateral substrate portion **64**, thus containing the heat generated by the channel region and allowing it to be better route the heat to the object to be heated.

[0051] In this seventh alternative embodiment of **FIG. 8**, the dielectric layer **24** extends laterally over the lateral substrate portion **64**, and an overlay dielectric layer **66** extends over the dielectric layer **50**. The overlay dielectric layer **66** is selected with thermal insulating properties to limit the amount of the heat **22** generated by the channel region **20** that is transferred therethrough, and for passivation to protect the gate electrode **26** and the contacts **14***a* and **16***a* used for the source and drain regions **14** and **16**. A window **68** is formed in the overlay dielectric layer **66** at a location laterally offset from the MOSFET and corresponding to the lateral substrate portion **64**. A body **70** made of silicon with a wall portion **72** defines the chamber **30** with an inward opening **74** and an orifice **76** through which the substance **32** can pass, such as a fluid. The wall portion **72** of the body **70** is positioned adjacent to and in sealing engagement with the overlay dielectric layer **66**, with the inward opening **74** of the chamber **30** in alignment with the window **68** so that the heat **22** generated by the channel region **20** which is transmitted laterally through the lateral substrate portion **64** will pass through the window and into the chamber.

[0052] An eighth alternative embodiment of the heater **10** is shown in **FIG. 9**. The heater **10** of **FIG. 9** has the same basic construction as the heater of **FIG. 8** and has the chamber **30** is located on the front of the wafer **11**'. However, instead of the substrate **12** and the body **52** extending laterally and providing a window in the overlay dielectric layer **66**, in this eighth alternative embodiment the chamber **30** formed by the wall portion **72** of the body **70** has the inward opening **74** positioned immediately over the MOSFET. Further, the inward opening **74** has sufficiently large lateral sized to span the source and drain regions **14** and **16**, the gate electrode **26** and the channel region **20**, and terminates above the trench **60** formed in the substrate **12** which is located laterally outward of and extends fully about the source and drain regions **14** and **16** and channel region **20**. In such manner, the heat **22** generated by the channel region **20** is thermally blocked by the oxide layer **50** and the trench **60**, and thus contained within the wall portion **34** of the substrate**12** inward of the oxide layer **50** and the trench **60**, and transmitted through the gate electrode **26** and the overlay dielectric layer **66** around the gate electrode. The heat **22** is then passed through the inward opening **74** and into the chamber **30**. In this embodiment, the overlay dielectric layer **66** is selected with thermal properties which allow sufficient amount of the heat **22** generated by the channel region **20** to be transferred through the overlay dielectric layer as needed to supply the desired heat to the chamber **30** and to whatever substance may be therein.

[0053] To improve the efficiency of the heater **10**, the gate electrode **26** used in this eighth alternative embodiment may be fabricated using a material that provides a desirable thermal conductivity for the application for which the heater is to be used. Also, the gate material may be selected to provide a long mechanical life. In an inkjet printhead, a material can be selected for the gate electrode **26** that can withstand the high pressures encountered with heated ink and the cavitation effect that is so damaging to prior art inkjet printhead component. The gate material can also be selected to avoid damage that might come from contact of the fluid with the gate electrode **26**, should such occur. A metal, such as tantalum, tantalum alloy, aluminum and aluminum alloy are acceptable for the gate electrode **26**. In this invention, it may be desirable to use a metal gate electrode and have the appropriate thickness gate dielectric, whether an oxide or nitride or sandwich thereof, to provide reliable, long-term operation for many applications.

[0054] The wafer **11** or **11**' on which the heater **10**, or more likely many heaters of the design desired for the application, may also contain MOSFETs or other circuitry that serves to control the heater MOSFETs as well as perform other functions. By putting the heater MOSFETs and the other MOSFETs on the same wafer or chip that is produced therefrom, cost savings and size advantages can be achieved. In such an arrangement, the heater MOSFETs and the other MOSFETs would be geometrically isolated from each other sufficiently that the channel regions of the two types of MOSFETs can be processed differently, with the channel region **20** of the heater MOSFETs being fabricated to enhance its channel resistance R_{DS} so as to produced the desired heat.

[0055] From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

1. An integrated heater comprising:

a semiconductor material;

at least one transistor formed in the semiconductor material and operable to generate heat above a selected threshold; and

an object to be heated positioned adjacent to the transistor to receive the heat generated by the transistor.

2. The integrated heater of claim 1 wherein the object to be heated is a fluid chamber positioned adjacent to the semiconductor material.

3. The integrated heater of claim 1 wherein the object to be heated is a fluid chamber formed in the semiconductor material.

4. The integrated heater of claim 1 wherein the semiconductor material has a wall portion adjacent to the transistor to transmit heat generated by the transistor through the semiconductor wall portion, and further including a body having wall portion positioned adjacent to and in sealing engagement with the semiconductor wall portion, such that the semiconductor wall portion and the body wall portion together define a fluid chamber as the object to be heated.

5. The integrated heater of claim 4, further including a dielectric layer extending over the semiconductor wall portion and facing toward the fluid chamber.

6. The integrated heater of claim 1, further including a thermally insulating barrier formed in the semiconductor material extending about the transistor to limit transmission in the semiconductor material of the heat generated by the transistor beyond the insulating barrier.

7. The integrated heater of claim 1 wherein the semiconductor material extends laterally beyond the transistor to provide a lateral semiconductor portion, and the object to be heated is positioned laterally adjacent to the transistor and adjacent to the lateral semiconductor portion to receive the heat generated by the transistor which is transmitted laterally to the lateral semiconductor portion.

8. The integrated heater of claim 7, further including a dielectric layer extending over the semiconductor material with a window formed in a portion of the dielectric layer at a location adjacent to the lateral semiconductor portion, and wherein the object to be heated is positioned at the window to receive the heat generated by the transistor which passes through the window.

9. The integrated heater of claim 7 wherein the object to be heated is a fluid chamber.

10. The integrated heater of claim 7 wherein the lateral semiconductor portion has a wall portion to transmit heat to the object to be heated that is generated by the transistor and transmitted through the lateral semiconductor portion, and further including a body having a wall portion positioned adjacent to and in sealing engagement with the lateral semiconductor wall portion, such that the lateral semiconductor wall portion and the body wall portion together define a fluid chamber as the object to be heated.

11. The integrated heater of claim 7, further including a thermally insulating barrier formed in the semiconductor material extending laterally outward of and about the transistor and the lateral semiconductor portion to limit transmission in the semiconductor material of the heat generated by the transistor laterally beyond the insulating barrier.

12. The integrated heater of claim 7, further including has a dielectric layer extending over a first face of the semiconductor material and a window formed in a portion of the dielectric layer over the lateral semiconductor portion, with the object to be heated positioned at the window to receive the heat generated by the transistor which passes through the window, and further including a thermally insulating barrier formed in the semiconductor material extending laterally outward of and about the transistor and the window to limit transmission in the semiconductor material of the heat generated by the transistor laterally beyond the insulating barrier.

13. The integrated heater of claim 12, further including a thermally insulating layer extending over a second face of the semiconductor material opposite the first face, and the insulating barrier is positioned between the dielectric layer and the insulating layer.

14. The integrated heater of claim 12 wherein the object to be heated is a fluid chamber.

15. The integrated heater of claim 12, further including a body having wall portion positioned adjacent to and in sealing engagement with the dielectric layer about the window, such that the body wall portion defines a fluid chamber as the object to be heated with the heat being supplied thereto through the window.

16. The integrated heater of claim 1, further including a dielectric layer extending over a first face of the semiconductor material with the object to be heated positioned adjacent to the dielectric layer on a side thereof opposite the transistor to receive the heat generated by the transistor.

17. The integrated heater of claim 16, further including a thermally insulating barrier formed in the semiconductor material to define a portion of the semiconductor material inward to the insulating barrier positioned to receive the heat generated by the transistor, the insulating barrier being of a material which limits transmission of the heat generated by the transistor and received by the inward portion of the semiconductor material beyond the insulating barrier.

18. The integrated heater of claim 16, further including a thermally insulating layer extending over a second face of the semiconductor material opposite the first face.

19. The integrated heater of claim 16, further including a body having a wall portion positioned adjacent to and in sealing engagement with the dielectric layer, such that the dielectric layer and the body wall portion together define a fluid chamber as the object to be heated.

20. The integrated heater of claim 1 wherein the object to be heated is a fluid.

21. An integrated heater comprising:

a semiconductor material;

a plurality of transistors formed in the semiconductor material and selectively operable to generate heat; and

an object to be heated positioned adjacent to the transistors to receive the heat generated by the transistors.

22. The integrated heater of claim 21 wherein the object to be heated is a fluid chamber positioned adjacent to the semiconductor material.

23. The integrated heater of claim 21, further including a thermally insulating barrier formed in the semiconductor material extending a perimeter about the transistors to limit transmission of the heat generated by the transistors beyond the insulating barrier.

24. An integrated heater comprising:

a semiconductor substrate;

a source region disposed in the semiconductor substrate;

a drain region disposed in the semiconductor substrate;

a channel region disposed in the semiconductor substrate between the source and drain regions to conduct electric current between the source and drain regions, the channel region having a resistance when conducting current to generate heat above a selected threshold;

a dielectric layer disposed on the channel region;

a gate electrode disposed on the dielectric layer to control the current conducted by the channel region; and

an object to be heated positioned to receive the heat generated by the resistance of the channel region.

25. The integrated heater of claim 24 wherein the object to be heated is a fluid chamber positioned adjacent to the semiconductor material.

26. The integrated heater of claim 24 wherein the object to be heated is a fluid chamber formed in the semiconductor substrate.

27. The integrated heater of claim 24, further including a thermally insulating barrier formed in the semiconductor substrate and extending at least partially about the channel region to define a portion of the semiconductor substrate inward to the insulating barrier positioned to receive the heat generated by the resistance of the channel region.

28. The integrated heater of claim 24 wherein the semiconductor substrate has a wall portion adjacent to the channel region to transmit the heat generated by the resistance of the channel region through the semiconductor wall portion, and further including a body having a wall portion positioned adjacent to the semiconductor wall portion and defining a fluid chamber as the object to be heated.

29. The integrated heater of claim 28, further including a heat transmitting dielectric layer positioned between the semiconductor wall portion and the body wall portion.

30. The integrated heater of claim 24, further including a body having a wall portion positioned adjacent to the dielectric layer and defining a fluid chamber as the object to be heated.

31. The integrated heater of claim 24, further including a thermally insulating layer positioned toward a side of the semiconductor substrate away from the dielectric layer.

32. The integrated heater of claim 31, further including a thermally insulating barrier formed in the semiconductor substrate to define an inward portion of the semiconductor substrate inward of the insulating barrier and positioned to receive the heat generated by the resistance of the channel region, the insulating barrier being of a material which limits transmission of the heat generated by the resistance of the channel region and received by the inward portion of the semiconductor material beyond the insulating barrier, the object to be heated being in thermal communication with the inward portion of the semiconductor material.

33. The integrated heater of claim 32 wherein the insulating barrier projects substantially fully between the dielectric layer and the insulating layer.

34. The integrated heater of claim 24, further including an overlay dielectric layer overlaying the gate electrode, the object to be heated being positioned adjacent to the overlay dielectric layer.

35. The integrated heater of claim 34, further including a body having a wall portion positioned adjacent to the overlay dielectric layer, across from the gate electrode, and defining a fluid chamber as the object to be heated.

36. The integrated heater of claim 35, further including a thermally insulating barrier formed in the semiconductor substrate and extending at least partially about the channel region to define a portion of the semiconductor substrate inward of the insulating barrier and adjacent to the fluid chamber such that the inward portion of the semiconductor substrate is in thermal communication with the fluid chamber.

37. The integrated heater of claim 36, further including a thermally insulating layer positioned toward a side of the semiconductor substrate away from the dielectric layer.

38. The integrated heater of claim 37 wherein the insulating barrier projects substantially fully between the dielectric layer and the insulating layer.

39. The integrated heater of claim 24 wherein the semiconductor substrate extends laterally beyond the source and drain regions to provide a lateral semiconductor substrate portion, and the object to be heated is positioned adjacent to the lateral semiconductor substrate portion to receive the heat generated by the resistance of the channel region which is transmitted laterally thereto through the lateral semiconductor substrate portion.

40. The integrated heater of claim 39, wherein the dielectric layer extends laterally over the lateral semiconductor substrate portion, and further including an overlay dielectric layer overlaying the gate electrode and a window formed in of the overlay dielectric layer at a location corresponding to the lateral semiconductor substrate portion, and wherein the object to be heated is positioned at the window to receive the heat transmitted laterally through the lateral semiconductor substrate portion generated by the resistance of the channel region and which passes through the window.

41. The integrated heater of claim **40**, further including a body having a wall portion positioned adjacent to the window and defining a fluid chamber as the object to be heated with the heat being supplied thereto through the window.

42. The integrated heater of claim 24 wherein the gate electrode is metal.

43. The integrated heater of claim 24 wherein the object to be heated is a fluid.

* * * * *

Appendix B

US006160243A

United States Patent [19]

Cozad

[11] Patent Number: 6,160,243

[45] Date of Patent: Dec. 12, 2000

[54] **APPARATUS AND METHOD FOR CONTROLLING FLUID IN A MICROMACHINED BOILER**

[75] Inventor: **Bradford Allen Cozad**, Newark, Calif.

[73] Assignee: **Redwood Microsystems, Inc.**, Menlo Park, Calif.

[21] Appl. No.: **09/161,185**

[22] Filed: **Sep. 25, 1998**

[51] **Int. Cl.**[7] **F27D 11/00**; F16K 31/00

[52] **U.S. Cl.** **219/439**; 251/11

[58] **Field of Search** 219/439, 438, 219/436, 432, 407; 204/601; 251/11; 137/505, 501; 430/326; 60/512; 392/439, 304

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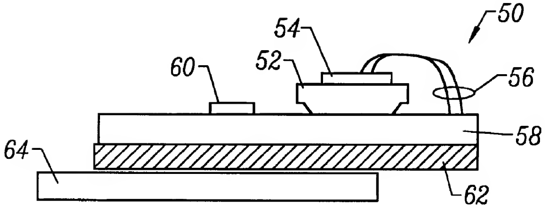
Primary Examiner—Teresa Walberg
Assistant Examiner—Daniel Robinson
Attorney, Agent, or Firm—William S. Galliani; Pennie & Edmonds LLP

[57] **ABSTRACT**

A micromachined fluid control apparatus includes a micromachined boiler with a thermally conductive housing that has a housing exterior surface and a housing interior surface. The housing interior surface defines an interior void that has a fluid positioned within it. A heat source is incorporated with the housing exterior surface. The heat source selectively generates heat that is conducted through the thermally conductive housing so as to selectively expand the fluid in a predetermined manner. A load resistor may be positioned within the thermally conductive housing. Current may be driven through the load resistor in a predetermined manner to further control the selective expansion of the fluid.

12 Claims, 5 Drawing Sheets



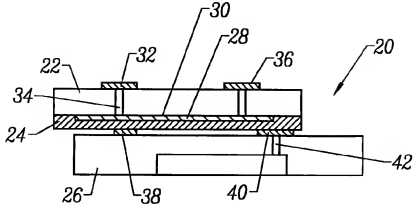


FIG. 1
(PRIOR ART)

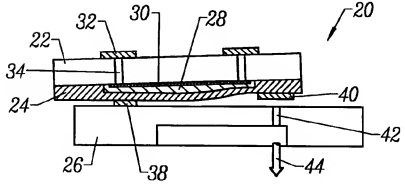


FIG. 2
(PRIOR ART)

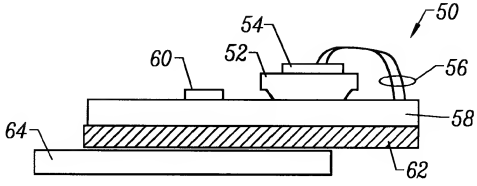


FIG. 3

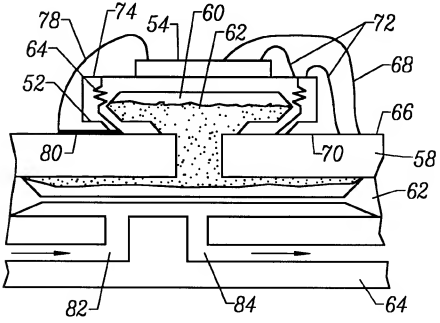


FIG. 4

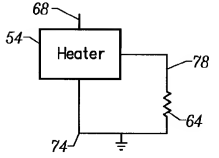


FIG. 5

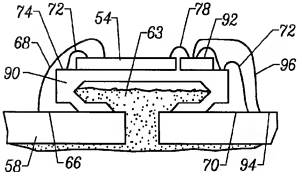


FIG. 6

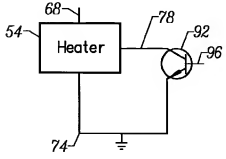


FIG. 7

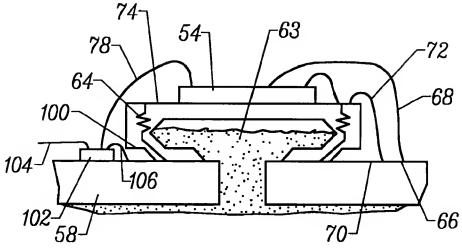


FIG. 8

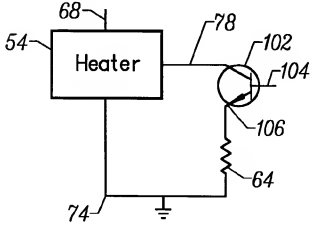


FIG. 9

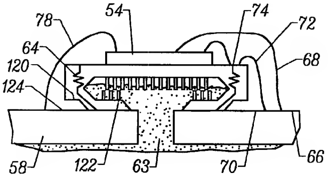


FIG. 10

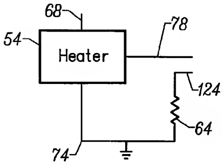


FIG. 11

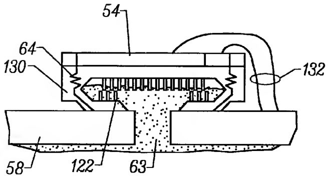


FIG. 12

APPARATUS AND METHOD FOR CONTROLLING FLUID IN A MICROMACHINED BOILER

BRIEF DESCRIPTION OF THE INVENTION

This invention relates generally to micromachined fluid control devices, such as valves and pumps. More particularly, this invention relates to a thermally conductive boiler controlled by a heat source positioned outside of the boiler chamber.

BACKGROUND OF THE INVENTION

Micromachined devices (also called micromechanical devices or microelectro-mechanical devices) are small (micron scale) machines that are constructed using semiconductor processing techniques. Micromachines include a variety of devices, such as fluid control devices (e.g., valves and pumps), motors, and gear trains analogous to conventional macroscale machinery. As used herein, the term micromachine refers to any three-dimensional object that is at least partially constructed in reliance upon semiconductor processing techniques.

FIG. **1** illustrates a micromachined valve **20** constructed in accordance with the prior art. The valve **20** includes three major components: a heat insulating substrate **22**, a deformable membrane **24**, and a fluid routing substrate **26**. The heat insulating substrate **22** may be formed of Pyrex, while the deformable membrane may be formed of silicon. A working fluid **28** is positioned in a void formed between the heat insulating substrate **22** and the deformable membrane **24**. A thin-film heater **30** is formed on the heat insulating substrate **22**. More particularly, as shown in FIG. **1**, the thin-film heater **30** is attached to an interior surface of the valve **20**. An electrical contact **32** and an electrical feedthrough **34** are used to supply current to the thin-film heater **30**. Although not shown for the purpose of simplicity, at least one additional contact and electrical feedthrough are also used. FIG. **1** also shows a seal cap **36** which may be used to deliver the working fluid **28** into the valve **20**.

The deformable membrane **24** is positioned on a pedestal **38** and carries a valve seat **40**. The valve seat **40** rests over a valve opening **42**. Thus, the apparatus of FIG. **1** represents a normally closed valve. That is, the valve of FIG. **1** is closed when no power is applied to it.

FIG. **2** illustrates the valve of FIG. **1** in an open state after power is applied to it. When current is applied across the thin-film resistor **30**, the working fluid **28** is heated and subsequently expands, thereby deforming the deformable membrane **24**. As a result, fluid can pass through the valve opening **42**, as shown with arrow **44**.

Those skilled in the art will recognize a number of shortcomings associated with the apparatus of FIGS. **1** and **2**. First, the prior art device is relatively slow because it is relatively time-consuming to heat the working fluid **28** with the thin-film heater **30**. In addition, the prior art device is relatively expensive to manufacture and test. A significant portion of this expense is associated with the thin-film heater **30**. The thin-film heater **30** is inherently expensive to manufacture. Testing of the thin-film structure is difficult because of the position of the thin-film heater in the interior of the valve. Furthermore, it is relatively expensive to provide a thin-film heater with refined temperature and current control capabilities.

In view of the foregoing, it would be highly desirable to provide an improved micromachined fluid control device.

Such a device should provide improved speed in controlling the temperature of the working fluid. In addition, such a device should be relatively inexpensive to manufacture and test.

SUMMARY OF THE INVENTION

The apparatus of the invention is a micromachined boiler with a thermally conductive housing that has a housing exterior surface and a housing interior surface. The housing interior surface defines an interior void that has a fluid positioned within it. A heat source is incorporated with the housing exterior surface. The heat source selectively generates heat that is conducted through the thermally conductive housing so as to selectively expand the fluid in a predetermined manner. A load resistor may be positioned within the thermally conductive housing. Current may be driven through the load resistor in a predetermined manner to further control the selective expansion of the fluid.

The method of the invention includes the step of enclosing a working fluid within a micromachined boiler with a thermally conductive housing. The thermally conductive housing is subsequently heated to control the expansion of the working fluid within the micromachined boiler. Current may be selectively driven through a load resistor positioned within the thermally conductive housing to control the expansion of the working fluid within the micromachined boiler.

The combination of the thermally conductive boiler housing and externally positioned heat source provides rapid proportional control of the working fluid within the boiler. The heat source of the invention is relatively easy to assemble. The position of the heat source also facilitates testing. The heat source may be implemented as a low-cost, externally mounted controller. Alternately, the heat source may be integrally formed within the boiler. In either embodiment, the heat source is an external heat source since it is external to the interior of the boiler chamber. The thermally conductive housing efficiently exploits all thermal energy associated with the heat source.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the invention, reference should be made to the following detailed description taken in conjunction with the accompanying drawings, in which:

FIG. **1** illustrates a prior art valve that uses internal heating of a working fluid to control the valve state.

FIG. **2** illustrates the prior art valve of FIG. **1** in an open state.

FIG. **3** illustrates a micromachined fluid control apparatus in accordance with an embodiment of the invention.

FIG. **4** is an enlarged cross-sectional view of a micromachined fluid control apparatus in accordance with an embodiment of the invention.

FIG. **5** illustrates an electrical circuit corresponding to the apparatus of FIG. **4**.

FIG. **6** is an enlarged cross-sectional view of a micromachined fluid control apparatus in accordance with another embodiment of the invention.

FIG. **7** illustrates an electrical circuit corresponding to the apparatus of FIG. **6**.

FIG. **8** is an enlarged cross-sectional view of a micromachined fluid control apparatus in accordance with another embodiment of the invention.

FIG. **9** illustrates an electrical circuit corresponding to the apparatus of FIG. **8**.

FIG. 10 is an enlarged cross-sectional view of a micromachined fluid control apparatus in accordance with another embodiment of the invention.

FIG. 11 illustrates an electrical circuit corresponding to the apparatus of FIG. 10.

FIG. 12 illustrates a micromachined fluid control apparatus in accordance with another embodiment of the invention.

Like reference numerals refer to corresponding parts throughout the drawings.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 3 illustrates a micromachined fluid control apparatus **50** in accordance with an embodiment of the invention. The apparatus **50** includes a micromachined boiler **52**. The micromachined boiler **52** includes a thermally conductive housing that defines an interior void (shown in subsequent figures). A heat source **54** is incorporated with the exterior of the micromachined boiler **52**. The heat source **54** may either be a discrete device attached to the boiler **52**, as shown in FIG. **3**, or it may be a device integrated into the boiler. In either embodiment, the heat source is external to the interior chamber defined by the boiler. Heater bond wires **56** are attached to the heat source **54**.

The micromachined boiler **52** is preferably positioned on an insulating substrate **58**, which may have a fluid seal cap **60**. The insulating substrate may be formed of Pyrex. A deformable membrane **62** is attached to the insulating substrate **58**. By way of example, the deformable membrane **62** may be formed of silicon. A fluid routing substrate **65** is attached to the deformable membrane **62**. The deformable membrane **62**, the fluid routing substrate **65**, and the insulating substrate **58** may be of the type known in the art. The invention is directed toward the micromachined boiler **52** and its associated heater **54**. Those skilled in the art will appreciate that any number of valve configurations or other external devices may be utilized in connection with the disclosed boiler **52**.

The micromachined boiler **52** is formed of a thermally conductive material. As used herein, the term thermally conductive material refers to a material with a thermal conductivity of at least 40 W/m K, preferably at least 80 W/m K. The invention has been implemented with a silicon micromachined boiler **52**. In this embodiment, standard semiconductor processing techniques are used to fabricate individual halves of the boiler cylinder. As discussed below, a load resistor may be formed within the individual halves of the cylinder, or may be placed at the interface between the halves. The load resistor may be an implanted device, a thin-film device, or the like. The individual halves are sealed to form a closed chamber.

The external heater **54** provides a resistive heat source. Preferably, the external heater **54** includes a control circuit to reduce heat output from the heater **54** when the heat output reaches a predetermined temperature. Alternately, the external heater **54** includes a control circuit to reduce current flow through the heater **54** when the current flow reaches a predetermined value. By way of example, the external heater **54** has been implemented with a MC7805 integrated circuit sold by Motorola, Inc., Schaumburg, Ill.

Those skilled in the art will recognize a number of benefits associated with the apparatus of FIG. **3**. First, the boiler **52** is completely formed from a thermally conductive material. Thus, any heat associated with the heater **54** is conveyed to the working fluid within the boiler **52**. This results in rapid heating of the working fluid. Observe that with the apparatus of FIGS. **1** and **2**, the thin-film heater **30** is formed on an insulating substrate 22.

The apparatus **50** of FIG. **3** is also advantageous because it uses an externally positioned heater **54**. A discrete external heater provides a low-cost implementation. An integrated external heater provides a compact and efficient implementation.

The operation and benefits of the invention are more fully appreciated with reference to FIG. 4. FIG. **4** is an enlarged cross section of the "normally open" embodiment of the device. The figure illustrates the boiler **52**, which defines a boiler chamber **61**. A working fluid **63** is positioned within the chamber **61**. In the embodiment of FIG. **4**, a load resistor **64** is positioned within the wall of the boiler **52**.

A voltage input bond pad **66** is positioned on the insulating substrate **58**. A voltage input bond wire **68** extends from the bond pad **66** to the top of the heater **54**. A ground bond pad **70** is also positioned on the insulating substrate **58**. Ground bond wires **72** are attached to the boiler **52** and the heater **54**. A ground plane **74** is formed on the top of the boiler **52**. An output bond wire **78** extends from the top of the heater **54** to an output lead **80**, which is electrically linked with the load resistor **64**.

FIG. **5** illustrates an electrical circuit corresponding to the device of FIG. **4**. FIG. **5** illustrates the voltage input bond wire **68** being applied to the heater **54**. The output bond wire **78** from the heater is connected to the load resistor **64**, which is connected to ground at its other end. The heater **54** is also grounded via the ground bond wire **72**. The input voltage applied from node **68** is applied to the heater **54**, causing the heater to generate resistive heat, which is conducted to the working fluid **63**. Resistive heat is also generated by the load resistor **64**.

The applied heat causes the working fluid **63** to expand. As a result, the deformable membrane **62** distends to block the output port **84** of the fluid routing substrate **64**. Control of the working fluid **63** provides proportional control of the valve. Those skilled in the art will appreciate that the boiler of the invention can be used with any number of fluid control paths, valves, or pumps. The configuration of FIG. **4** is solely provided by way of example.

FIG. **6** illustrates another embodiment of the micromachined boiler of the invention. The apparatus of FIG. **6** does not include a load resistor. Instead, a load transistor **92** is provided. The transistor is used as a load and a secondary heating source. The load transistor **92** allows dynamic output loading. The transistor **92** may be mounted onto the boiler **54**, manufactured into the boiler **54**, or mounted remotely.

The boiler **90** of FIG. **6** encloses a working fluid **63**. The boiler **90** is positioned on an insulating substrate **58**. A voltage input bond pad **66** is positioned on the substrate **58**. A voltage input bond wire **68** extends from the bond pad **66** to the top of the heater **54**. A ground bond pad **70** is also positioned on the substrate **58**. Ground bond wires **72** extend to the ground plane **74**, the load transistor **92**, and the heater **54**. The load transistor **92** is connected to a control input pad **94** via a control input bond wire **96**. An output bond wire **78** links an output node of the heater **54** to the load transistor **92**.

FIG. **7** illustrates an electrical circuit corresponding to the device of FIG. **6**. An output node of the heater **54** is connected to the load transistor **92**. The control input bond wire **96** is attached to the gate or base of the transistor **92**. In this embodiment, the heater **54** provides heat to the working fluid, as does the transistor **92**.

FIG. **8** illustrates another embodiment of the invention. In this embodiment, the boiler **100** includes an internal load

resistor **64** and an externally mounted transistor **102**. FIG. **9** is a schematic corresponding to the device of FIG. **8**. A control input bond wire **104** is attached to the gate or base of transistor **102**. A transistor output lead **106** is electrically connected to the load resistor **64**. Thus, in this embodiment, the transistor **102** is used as a power control device, allowing for fast, efficient heating.

FIG. **10** illustrates still another embodiment of the invention. In this embodiment, the boiler **120** includes a set of heat transfer fins **122** positioned within the boiler interior chamber. The heat transfer fins **122** improve the heat transfer characteristics of the device. A separate resistor input lead **124** is provided in this embodiment to establish separate control of the load resistor **64**. FIG. **11** illustrates an electrical schematic corresponding to the device of FIG. **10**.

FIG. **12** illustrates a boiler **130** in which the heater **54** is integral with the boiler housing. Bond wires **132** are used to establish the required electrical connections. The device of FIG. **12** operates consistently with the previously disclosed embodiments of the invention.

The foregoing description, for purposes of explanation, used specific nomenclature to provide a thorough understanding of the invention. However, it will be apparent to one skilled in the art that the specific details are not required in order to practice the invention. In other instances, well known circuits and devices are shown in block diagram form in order to avoid unnecessary distraction from the underlying invention. Thus, the foregoing descriptions of specific embodiments of the present invention are presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed. Obviously, many modifications and variations are possible in view of the above teachings. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the following Claims and their equivalents.

What is claimed is:

1. A micromachined fluid control apparatus, comprising:

a micromachined boiler including a thermally conductive housing with a housing exterior surface and a housing interior surface defining an interior void with a fluid positioned therein; and

a heat source positioned on said housing exterior surface, said heat source selectively generating heat that is conducted through said thermally conductive housing to selectively expand said fluid in a predetermined manner to control fluid flow;

wherein said thermally conductive housing includes a plurality of heat transfer fins positioned within said interior void.

2. The micromachined fluid control apparatus of claim **1** wherein said heat source is a discrete device positioned on said housing exterior surface.

3. The micromachined fluid control apparatus of claim **1** wherein said thermally conductive housing is formed of silicon.

4. The micromachined fluid control apparatus of claim **1** wherein said thermally conductive housing has a load resistor positioned therein.

5. The micromachined fluid control apparatus of claim **1** wherein said heat source is a resistive heat source.

6. The micromachined fluid control apparatus of claim **4** wherein said heat source is a resistive heat source and is electrically connected to said load resistor such that said load resistor generates heat within said thermally conductive housing.

7. The micromachined fluid control apparatus of claim **1** wherein said heat source includes a control circuit to reduce heat output from said heat source when said heat source reaches a predetermined temperature.

8. The micromachined fluid control apparatus of claim **1** wherein said heat source includes a control circuit to reduce current flow through said heat source when current flow in said heat source reaches a predetermined value.

9. The micromachined fluid control apparatus of claim **4** further comprising a transistor to control the current driven through said load resistor and thereby control heat that is applied to said fluid within said interior void.

10. The micromachined fluid control apparatus of claim **1** further comprising an insulating substrate attached to said micromachined boiler, said insulating substrate including an aperture in fluid communication with said interior void of said housing interior surface.

11. The micromachined fluid control apparatus of claim **10** further comprising a deformable membrane attached to said insulating substrate.

12. The micromachined fluid control apparatus of claim **11** further comprising a fluid routing substrate attached to said deformable membrane, said fluid from said boiler selectively pressing against said deformable membrane to obstruct flow of a controlled fluid within said fluid routing substrate.

* * * * *

Appendix C

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MOTOROLA

Three-Terminal Positive Voltage Regulators

MC7800, MC7800A, LM340, LM340A Series

THREE–TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

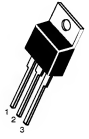
SEMICONDUCTOR TECHNICAL DATA

These voltage regulators are monolithic integrated circuits designed as fixed–voltage regulators for a wide variety of applications including local, on–card regulation. These regulators employ internal current limiting, thermal shutdown, and safe–area compensation. With adequate heatsinking they can deliver output currents in excess of 1.0 A. Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents.

- Output Current in Excess of 1.0 A
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation
- Output Voltage Offered in 2% and 4% Tolerance
- Available in Surface Mount D^2PAK and Standard 3–Lead Transistor Packages
- Previous Commercial Temperature Range has been Extended to a Junction Temperature Range of –40°C to +125°C

T SUFFIX
PLASTIC PACKAGE
CASE 221A

Heatsink surface connected to Pin 2.



Pin 1. Input
2. Ground
3. Output

D2T SUFFIX
PLASTIC PACKAGE
CASE 936
(D^2PAK)

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

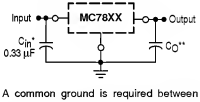
MC7805AC LM340AT–5	5.0 V	MC7812C LM340T–12	12 V
MC7805C LM340T–5		MC7815AC LM340AT–15	15 V
MC7806AC MC7806C	6.0 V	MC7815C LM340T–15	
MC7808AC MC7808C	8.0 V	MC7818AC MC7818C	18 V
MC7809C	9.0 V	MC7824AC MC7824C	24 V
MC7812AC LM340AT–12	12 V		

ORDERING INFORMATION

Device	Output Voltage Tolerance	Operating Temperature Range	Package
MC78XXACT	2%	T_J = –40° to +125°C	Insertion Mount
LM340AT–XX			
MC78XXACD2T			Surface Mount
MC78XXCT	4%		Insertion Mount
LM340T–XX			
MC78XXCD2T			Surface Mount

XX indicates nominal voltage.

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX, These two digits of the type number indicate nominal voltage.

* C_{in} is required if regulator is located an appreciable distance from power supply filter.

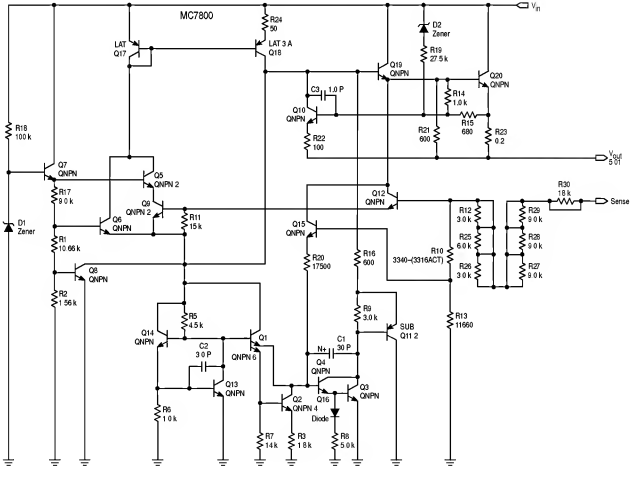
** C_O is not needed for stability; however, it does improve transient response. Values of less than 0.1 µF could cause instability.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 – 18 V) (24 V)	V_I	35 40	Vdc
Power Dissipation Case 221A T_A = 25°C Thermal Resistance, Junction–to–Ambient Thermal Resistance, Junction–to–Case Case 936 (D^2PAK) T_A = 25°C Thermal Resistance, Junction–to–Ambient Thermal Resistance, Junction–to–Case	 P_D $R_{\theta JA}$ $R_{\theta JC}$ P_D $R_{\theta JA}$ $R_{\theta JA}$	 Internally Limited 65 5.0 Internally Limited See Figure 13 5.0	 W °C/W °C/W W °C/W °C/W
Storage Junction Temperature Range	T_{Stg}	–65 to +150	°C
Operating Junction Temperature	T_J	+150	°C

NOTE: ESD data available upon request.

Representative Schematic Diagram



This device contains 22 active transistors.

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7805C/LM340T–5 Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	4.8	5.0	5.2	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W) 7.0 Vdc ≤ V_{in} ≤ 20 Vdc 8.0 Vdc ≤ V_{in} ≤ 20 Vdc	V_O	 4.75 –	 5.0 –	 5.25 –	Vdc
Line Regulation (Note 2) 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, 1.0 A 8.0 Vdc ≤ V_{in} ≤ 12 Vdc	Reg_{line}	 – –	 0.5 0.8	 20 10	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A (T_A = 25°C)	Reg_{load}	 – -	 1.3 1.3	 25 25	mV
Quiescent Current	I_B	–	3.2	6.5	mA
Quiescent Current Change 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A (T_A = 25°C)	ΔI_B	 – –	 0.3 0.08	 1.0 0.8	mA
Ripple Rejection 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz	RR	62	83	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.6	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.3	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7805AC/LM340AT–5 Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	4.9	5.0	5.1	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W) 7.5 Vdc ≤ V_{in} ≤ 20 Vdc	V_O	4.8	5.0	5.2	Vdc
Line Regulation (Note 2) 7.5 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 8.0 Vdc ≤ V_{in} ≤ 12 Vdc, I_O = 1.0 A 8.0 Vdc ≤ V_{in} ≤ 12 Vdc, I_O = 1.0 A, T_J = 25°C 7.3 Vdc ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A, T_J = 25°C	Reg_{line}	 – – – –	 0.5 0.8 1.3 4.5	 10 12 4.0 10	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – – –	 1.3 0.8 0.53	 25 25 15	mV
Quiescent Current	I_B	–	3.2	6.0	mA
Quiescent Current Change 8.0 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 0.3 – 0.08	 0.8 0.8 0.5	mA
Ripple Rejection 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, I_O = 500 mA	RR	68	83	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc

NOTES: 1. T_{low} = –40°C for MC78XXAC, C, LM340AT–XX, LM340T–XX T_{high} = +125°C for MC78XXAC, C, LM340AT–XX, LM340T–XX

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7805AC/LM340AT–5			Unit
		Min	Typ	Max	
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.3	–	mV/°C

NOTES: 1. T_{low} = –40°C for MC78XXAC, C, LM340AT–XX, LM340T–XX T_{high} = +125°C for MC78XXAC, C, LM340AT–XX, LM340T–XX

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7806C			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	5.75	6.0	6.25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W) 8.0 Vdc ≤ V_{in} ≤ 21 Vdc 9.0 Vdc ≤ V_{in} ≤ 21 Vdc	V_O	 5.7 –	 6.0 –	 6.3 –	Vdc
Line Regulation, T_J = 25°C (Note 2) 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 9.0 Vdc ≤ V_{in} ≤ 13 Vdc	Reg_{line}	 – –	 0.5 0.8	 24 12	mV
Load Regulation, T_J = 25°C (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A	Reg_{load}	–	1.3	30	mV
Quiescent Current (T_J = 25°C)	I_B	–	3.3	8.0	mA
Quiescent Current Change 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – –	 0.3 0.08	 1.3 0.5	mA
Ripple Rejection 9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz	RR	58	65	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I – V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.3	–	mV/°C

NOTES: 1. T_{low} = –40°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7806AC Min	MC7806AC Typ	MC7806AC Max	Unit
Output Voltage (T_J = 25°C)	V_O	5.88	6.0	6.12	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W) 8.6 Vdc ≤ V_{in} ≤ 21 Vdc	V_O	5.76	6.0	6.24	Vdc
Line Regulation (Note 2) 8.6 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 9.0 Vdc ≤ V_{in} ≤ 13 Vdc, I_O = 1.0 A	Reg_{line}	 – –	 5.0 1.4	 12 15	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – – –	 1.3 0.9 0.2	 25 25 15	mV
Quiescent Current	I_B	–	3.3	6.0	mA
Quiescent Current Change 9.0 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 9.0 Vdc ≤ V_{in} ≤ 21 Vdc, I_O = 1.0 A, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – – –	 0.8 0.8 0.5	mA
Ripple Rejection 9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz, I_O = 500 mA	RR	58	65	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.3	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7808C Min	MC7808C Typ	MC7808C Max	Unit
Output Voltage (T_J = 25°C)	V_O	7.7	8.0	8.3	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W) 10.5 Vdc ≤ V_{in} ≤ 23 Vdc	V_O	7.6	8.0	8.4	Vdc
Line Regulation, T_J = 25°C, (Note 2) 10.5 Vdc ≤ V_{in} ≤ 25 Vdc 11 Vdc ≤ V_{in} ≤ 17 Vdc	Reg_{line}	 – –	 6.0 1.7	 32 16	mV
Load Regulation, T_J = 25°C (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A	Reg_{load}	–	1.4	35	mV
Quiescent Current	I_B	–	3.3	8.0	mA
Quiescent Current Change 10.5 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – –	 – –	 1.0 0.5	mA
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz	RR	56	62	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O

NOTES: 1 T_{low} = –40°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C

2 Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 14 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7808C			Unit
		Min	Typ	Max	
Output Resistance f = 1.0 kHz	r_O	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.4	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7808AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	7.84	8.0	8.16	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W) 10.6 Vdc ≤ V_{in} ≤ 23 Vdc	V_O	7.7	8.0	8.3	Vdc
Line Regulation (Note 2) 10.6 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 11 Vdc ≤ V_{in} ≤ 17 Vdc, I_O = 1.0 A 10.4 Vdc ≤ V_{in} ≤ 23 Vdc, T_J = 25°C	Reg_{line}	 – – –	 6.0 1.7 5.0	 15 18 15	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – – –	 1.4 1.0 0.22	 25 25 15	mV
Quiescent Current	I_B	–	3.3	6.0	mA
Quiescent Current Change 11 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 10.6 Vdc ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – – –	 0.8 0.8 0.5	mA
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz, I_O = 500 mA	RR	56	62	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.4	–	mV/°C

NOTES: 1. T_{low} = –40°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 15 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7809CT			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	8.65	9.0	9.35	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W) 11.5 Vdc ≤ V_{in} ≤ 24 Vdc	V_O	8.55	9.0	9.45	Vdc
Line Regulation, T_J = 25°C (Note 2) 11 Vdc ≤ V_{in} ≤ 26 Vdc 11.5 Vdc ≤ V_{in} ≤ 17 Vdc	Reg_{line}	 – –	 6.2 1.8	 32 16	mV
Load Regulation, T_J = 25°C (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A	Reg_{load}	–	1.5	35	mV
Quiescent Current	I_B	–	3.4	8.0	mA
Quiescent Current Change 11.5 Vdc ≤ V_{in} ≤ 26 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – –	 – –	 1.0 0.5	mA
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz	RR	56	61	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	1.0	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.5	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7812C/LM340T–12			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	11.5	12	12.5	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W) 14.5 Vdc ≤ V_{in} ≤ 27 Vdc	V_O	11.4	12	12.6	Vdc
Line Regulation, T_J = 25°C (Note 2) 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 16 Vdc ≤ V_{in} ≤ 22 Vdc 14.8 Vdc ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A	Reg_{line}	 – – –	 3.8 0.3 –	 24 24 48	mV
Load Regulation, T_J = 25°C (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A	Reg_{load}	–	8.1	60	mV
Quiescent Current	I_B	–	3.4	6.5	mA
Quiescent Current Change 14.5 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A, T_J = 25°C 15 Vdc ≤ V_{in} ≤ 30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – – –	 0.7 0.8 0.5	mA
Ripple Rejection 15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz	RR	55	60	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc

NOTES: 1. T_{low} = –40°C for MC78XXAC, C, LM340AT–XX, LM340T–XX T_{high} = +125°C for MC78XXAC, C, LM340AT–XX, LM340T–XX

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 19 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7812C/LM340T–12			Unit
		Min	Typ	Max	
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	1.1	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.8	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7812AC/LM340AT–12			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	11.75	12	12.25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W) 14.8 Vdc ≤ V_{in} ≤ 27 Vdc	V_O	11.5	12	12.5	Vdc
Line Regulation (Note 2) 14.8 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 16 Vdc ≤ V_{in} ≤ 22 Vdc, I_O = 1.0 A 14.5 Vdc ≤ V_{in} ≤ 27 Vdc, T_J = 25°C	Reg_{line}	 – – –	 3.8 2.2 6.0	 18 20 120	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A	Reg_{load}	 – –	 – –	 25 25	mV
Quiescent Current	I_B	–	3.4	6.0	mA
Quiescent Current Change 15 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 14.8 Vdc ≤ V_{in} ≤ 27 Vdc, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A, T_J = 25°C	ΔI_B	 – – –	 – – –	 0.8 0.8 0.5	mA
Ripple Rejection 15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, I_O = 500 mA	RR	55	60	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I – V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	–	1.1	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.8	–	mV/°C

NOTES: 1. T_{low} = –40°C for MC78XXAC, C, LM340AT–XX, LM340T–XX T_{high} = +125°C for MC78XXAC, C, LM340AT–XX, LM340T–XX

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7815C/LM340T–15 Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	14.4	15	15.6	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W) 17.5 Vdc ≤ V_{in} ≤ 30 Vdc	V_O	14.25	15	15.75	Vdc
Line Regulation, T_J = 25°C (Note 2) 17.9 Vdc ≤ V_{in} ≤ 30 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc	Reg_{line}	 – –	 8.5 3.0	 30 28	mV
Load Regulation, T_J = 25°C (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A	Reg_{load}	–	1.8	55	mV
Quiescent Current	I_B	–	3.5	6.5	mA
Quiescent Current Change 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – – –	 0.8 0.7 0.5	mA
Ripple Rejection 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz	RR	54	58	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	1.2	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–1.0	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7815AC/LM340AT–15 Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	14.7	15	15.3	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W) 17.9 Vdc ≤ V_{in} ≤ 30 Vdc	V_O	14.4	15	15.6	Vdc
Line Regulation (Note 2) 17.9 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 20 Vdc ≤ V_{in} ≤ 26 Vdc 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A, T_J = 25°C	Reg_{line}	 – – –	 8.5 3.0 7.0	 20 22 20	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – – –	 1.8 1.5 1.2	 25 25 15	mV
Quiescent Current	I_B	–	3.5	6.0	mA
Quiescent Current Change 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – – –	 0.8 0.8 0.5	mA

NOTES: 1. T_{low} = –40°C for MC78XXAC, C, LM340AT–XX, LM340T–XX T_{high} = +125°C for MC78XXAC, C, LM340AT–XX, LM340T–XX

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 23 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7815AC/LM340AT–15			Unit
		Min	Typ	Max	
Ripple Rejection 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, I_O = 500 mA	RR	60	80	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	1.2	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–1.0	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7818C			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	17.3	18	18.7	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W) 21 Vdc ≤ V_{in} ≤ 33 Vdc	V_O	17.1	18	18.9	Vdc
Line Regulation, (Note 2) 21 Vdc ≤ V_{in} ≤ 33 Vdc 24 Vdc ≤ V_{in} ≤ 30 Vdc	Reg_{line}	 – –	 9.5 3.2	 50 25	mV
Load Regulation, (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A	Reg_{load}	–	2.0	55	mV
Quiescent Current	I_B	–	3.5	6.5	mA
Quiescent Current Change 21 Vdc ≤ V_{in} ≤ 33 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – –	 – –	 1.0 0.5	mA
Ripple Rejection 22 Vdc ≤ V_{in} ≤ 33 Vdc, f = 120 Hz	RR	53	57	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_{II} - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	1.3	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–1.5	–	mV/°C

NOTES: 1. T_{low} = –40°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7818AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	17.64	18	18.36	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W) 21 Vdc ≤ V_{in} ≤ 33 Vdc	V_O	17.3	18	18.7	Vdc
Line Regulation (Note 2) 21 Vdc ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA 24 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A 24 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A, T_J = 25°C 20.6 Vdc ≤ V_{in} ≤ 33 Vdc, I_O = 1.0 A, T_J = 25°C	Reg_{line}	 – – – –	 9.5 3.2 3.2 8.0	 22 25 10.5 22	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – – –	 2.0 1.8 1.5	 25 25 15	mV
Quiescent Current	I_B	–	3.5	6.0	mA
Quiescent Current Change 21 Vdc ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA 21.5 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – – –	 0.8 0.8 0.5	mA
Ripple Rejection 22 Vdc ≤ V_{in} ≤ 32 Vdc, f = 120 Hz, I_O = 500 mA	RR	53	57	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	1.3	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–1.5	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7824C			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	23	24	25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W) 27 Vdc ≤ V_{in} ≤ 38 Vdc	V_O	22.8	24	25.2	Vdc
Line Regulation, (Note 2) 27 Vdc ≤ V_{in} ≤ 38 Vdc 30 Vdc ≤ V_{in} ≤ 36 Vdc	Reg_{line}	 – –	 2.7 2.7	 60 48	mV
Load Regulation, (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A	Reg_{load}	–	4.4	65	mV
Quiescent Current	I_B	–	3.6	6.5	mA
Quiescent Current Change 27 Vdc ≤ V_{in} ≤ 38 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – –	 – –	 1.0 0.5	mA

NOTES: 1. T_{low} = –40°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 33 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7824C			Unit
		Min	Typ	Max	
Ripple Rejection 28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz	RR	50	54	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	1.4	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–2.0	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7824AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	23.5	24	24.5	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W) 27.3 Vdc ≤ V_{in} ≤ 38 Vdc	V_O	23.2	24	25.8	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
27 Vdc ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA		–	11.5	25	
30 Vdc ≤ V_{in} ≤ 36 Vdc, I_O = 1.0 A		–	3.8	28	
30 Vdc ≤ V_{in} ≤ 36 Vdc, T_J = 25°C		–	3.8	12	
26.7 Vdc ≤ V_{in} ≤ 38 Vdc, I_O = 1.0 A, T_J = 25°C		–	10	25	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C		–	2.1	15	
5.0 mA ≤ I_O ≤ 1.0 A		–	2.0	25	
250 mA ≤ I_O ≤ 750 mA		–	1.8	15	
Quiescent Current	I_B	–	3.6	6.0	mA
Quiescent Current Change	ΔI_B				mA
27.3 Vdc ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA		–	–	0.8	
27 Vdc ≤ V_{in} ≤ 38 Vdc, T_J = 25°C		–	–	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Ripple Rejection 28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz, I_O = 500 mA	RR	45	54	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	–	1.4	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–2.0	–	mV/°C

NOTES: 1. T_{low} = –40°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Figure 1. Peak Output Current as a Function of Input/Output Differential Voltage (MC78XXC, AC)

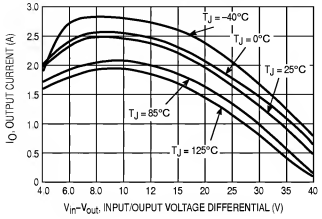


Figure 2. Ripple Rejection as a Function of Output Voltages (MC78XXC, AC)

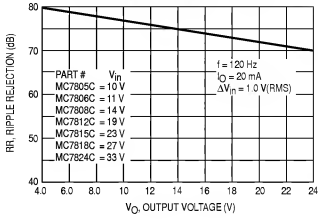


Figure 3. Ripple Rejection as a Function of Frequency (MC78XXC, AC)

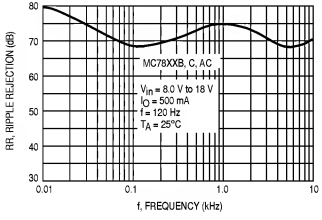


Figure 4. Output Voltage as a Function of Junction Temperature (MC7805C, AC)

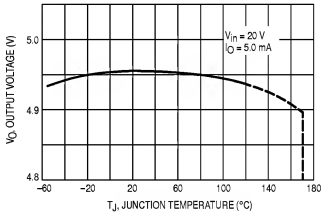


Figure 5. Output Impedance as a Function of Output Voltage (MC78XXC, AC)

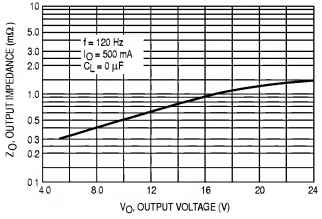
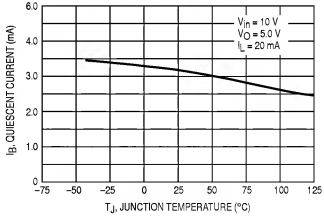


Figure 6. Quiescent Current as a Function of Temperature (MC78XXC, AC)

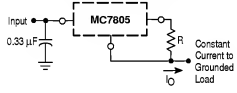


Design Considerations

The MC7800 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe–Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high–frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 7. Current Regulator



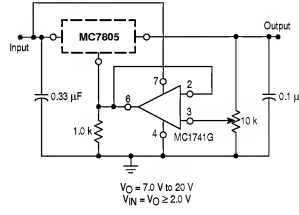
The MC7800 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

$I_B \cong 3.2$ mA over line and load changes.

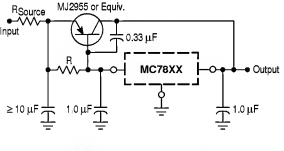
For example, a 1.0 A current source would require R to be a 5.0 Ω, 10 W resistor and the output voltage compliance would be the input voltage less 7.0 V.

Figure 8. Adjustable Output Regulator



The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 V greater than the regulator voltage.

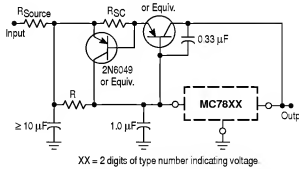
Figure 9. Current Boost Regulator



XX = 2 digits of type number indicating voltage.

The MC7800 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 A. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input/output differential voltage minimum is increased by V_{EC} of the pass transistor.

Figure 10. Short Circuit Protection



XX = 2 digits of type number indicating voltage.

The circuit of Figure 9 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three-terminal regulator. Therefore, a four–ampere plastic power transistor is specified.

Figure 11. Worst Case Power Dissipation versus Ambient Temperature (Case 221A)

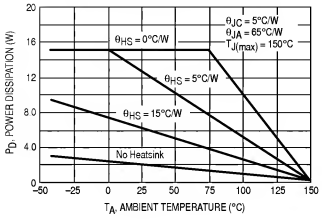


Figure 12. Input Output Differential as a Function of Junction Temperature (MC78XXC, AC)

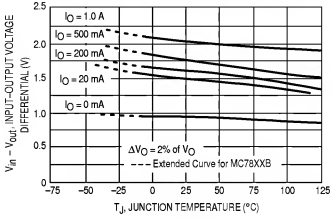
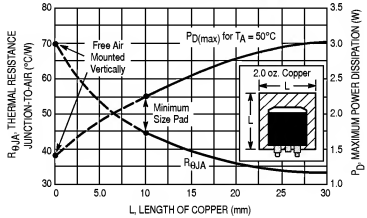


Figure 13. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

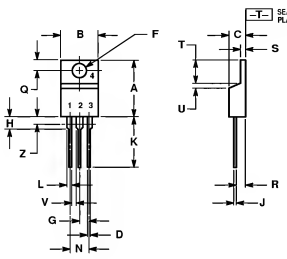
Quiescent Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

OUTLINE DIMENSIONS

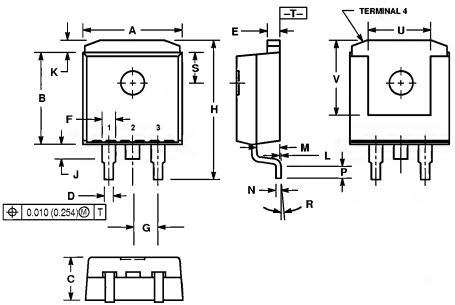
T SUFFIX
PLASTIC PACKAGE
CASE 221A–06
ISSUE Y



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	–	1.15	–
Z	–	0.080	–	2.04

D2T SUFFIX
PLASTIC PACKAGE
CASE 936–03
(D^2PAK)
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
F	0.051 REF		1.295 REF	
G	0.100 BSC		2.540 BSC	
H	0.539	0.579	13.691	14.707
J	0.125 MAX		3.175 MAX	
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.659
P	0.058	0.078	1.473	1.981
R	5° REF		5° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

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X. RELATED PROCEEDINGS APPENDIX

There are no proceedings related to the present appeal.

Respectfully submitted,

Seed Intellectual Property Law Group PLLC

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Registration No. 52,404

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